Rockchip RK1820 SODIMM Module Datasheet

Revision 1.0
August 2025

Revision History

Date	Revision	Description
2025-08-20	1.0	Initial release

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Chapter 1 Introduction

1.1 Overview

RK1820 SODIMM Module (Corresponding product name: RM1820SA0) is a high-performance AI co-processor module for machine vision application, especially for AI related application.

The RK1820 SODIMM Module is based on the RK1820 co-processor.

RK1820 is based on three 64-bit independent RISC-V cores with FPU. There is a 32KB I-cache,32KB D-cache and 128KB L2 cache for each core.

The built-in NPU Support INT4/INT8/INT16/FP8/FP16/BF16 hybrid operation and computing power is up to 20TOPS. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK1820 has an extreme high bandwidth built-in DRAM.

1.2 Features

1.2.1 RK1820 co-Processor

- Three RISC-V cores abbreviated as SRV, VRV0 and VRV1
- SRV is implemented with RV64GCB ISA and VR0/VRV1 is implemented with RV64GCBV ISA
- All cores are integrated FPU with RISC-V H/F/D precision
- Each core has 32KB L1 I-Cache, 32KB L1 D-Cache and 128KB L2 cache
- VRV0 and VRV1 is integrated with 128-bit vector unit

1.2.2 RK1820 Memory Organization

- RK1820 Internal on-chip memory
  - Bootrom
    - Support system boot from the following device:
      - FSPI interface
      - eMMC interface
      - SD/MMC interface
    - Support system code download by the following interface:
      - USB0 interface
      - UART0 interface
      - PCIe0 interface
  - 512KB system SRAM
  - Built-in Dynamic Memory Interface
    - Density is 2.5GB

- RK1820 External off-chip memory
  - Combo SDMMC Interface, work at only one of the following modes
    - eMMC
      - Fully compliant with JEDEC eMMC 4.51 specification
      - Support HS200, but not support CMD Queue
      - Support three data bus width mode: 1bit, 4bits and 8bits
    - SD/MMC Interface
      - Compatible with SD3.0, MMC ver4.51
      - Support 1bit, 4bits data bus width
    - Flexible Serial Flash Interface (SPI FLASH is on the module)

1.2.3 RK1820 System Component

- CRU (clock & reset unit)

- Support total 4 PLLs to generate all clocks
- One oscillator with 24MHz clock input
- Support clock gating control for individual components
- Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control
  - Support 3 separate voltage domains VDD_TOP, VDD_LOGIC, VDD_PMU

- Timer
  - Support 6 timers with 64bits counter and interrupt-based operation
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Three Watchdogs

- Interrupt Controller
  - Support 160 interrupt sources input from different components inside SoC for SRV and 64 interrupt sources input for VRV
  - Support 1 software-triggered interrupt in m-mode and s-mode each
  - Input interrupt level is fixed, high-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Support 2 physical channels
  - Support 22 groups of peripheral request interfaces
  - Support 24 logic channels, each logic channel support the following feature
    - Support the data transfer of memory-to-memory, memory-to-peripherals, peripherals-to-memory
    - Support Linked list DMA function to complete scatter-gather transfer
    - Support three kinds of multi-block transfer: contiguous address, auto reload, link list

- Secure System
  - Support one cipher engine
    - Support Symmetrical algorithms
      - AES-128, AES-192, AES-256, SM4
      - ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode for AES and SM4
    - Hash algorithm
      - SHA-1, SHA-256/224, MD5, SM3 with hardware padding
      - HMAC of SHA-1, SHA-256, MD5, SM3 with hardware padding
    - Asymmetrical algorithms
      - RSA (up to 4096 bits), ECC (up to 256 bits), SM2
    - Key-ladder (KL)
      - Support obtaining the root key from OTP or RKRNG and deriving it

- Support writes out root key or derived key to some specific modules
- Number of stages can be configured

- Mailbox
  - Twelve mailboxes in SoC used to service different RISC-V communication

1.2.4 RK1820 JPEG CODEC

- JPEG encoder
  - Supports Baseline (DCT sequential)
  - Supports JPEG file interchange format (JFIF) 1.02
  - Supports image size is from 16x16 to 65520x65520
  - Supports YUV400/YUV420/YUV422/YUV444

- JPEG Decoder
  - Support Baseline (DCT sequential)
  - Support JPEG file interchange format (JFIF) 1.02
  - Support image size is from 48x48 to 65520x65520
  - Support YUV400/YUV420/YUV422/YUV440/YUV411/YUV444/RG888/RGB565

1.2.5 RK1820 Neural Process Unit

- Rockchip NPU engine:
  - Up to 20 TOPS for INT8
  - Support INT4/INT8/INT16/FP8/FP16/BF16 operation
  - Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

1.2.6 RK1820 2D Graphics Engine

- 2D Graphics Engine (RGA)
- Data format
  - SRC0 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551
    - RGB888P/RGB565
    - YUV422-P/YUV422-SP-8bit/10bit (clip to 8bit after input)
    - YUV420-P/YUV420-SP-8bit/10bit (clip to 8bit after input)
    - YUV444I/YUV444SP-8bit
    - YVYU422-8bit
    - YUV400-8bit
    - TILE4X4 YUV420/422/444-8bit
    - TILE4X4 YUV420/422/444-10bit (clip to 8bit after input)
    - BPP1/2/4/8
  - SRC1 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
    - RGB888P/RGB565
  - Output data format (all YUV format is 8bit):
    - ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
    - RGB888/RGB565
    - YUV420/YUV422 P/SP
    - YUV400/Y4
    - YUV444SP/444I
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution : 8192x8192 source, 4096x4096 destination
- Scaling
  - Down-scaling: Average/Bilinear filter
  - Up-scaling: Bi-cubic filter(source>1992 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
  - 0, 90, 180, 270-degree rotation

- x-mirror, y-mirror operation
- Mirroring and rotation co-operation

- BitBLT
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT
  - A+B=B only BitBLT, A support rotate & scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- Alpha Blending
  - Comprehensive per-pixel alpha (color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y) +SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- OSD Automatic Inversion
  - Support OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
  - Support SRC0 and OSD overlay

1.2.7 RK1820 SODIMM Module Connectivity interface

- MAC 10/100/1000M Ethernet
  - Support one Ethernet controllers
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support both full-duplex and half-duplex operation
  - Support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO) network acceleration
  - Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008

- USB 2.0 DRD (Dual-Role Device)
  - Support one USB2.0 DRD (Dual-Role Device)
  - Compatible with USB 2.0 specification
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

- Multi-PHY Interface
  - Support two multi-PHY with two PCIe2.1 controller and one USB3.0 DRD controller (multiplex to one of the PHY)
  - Support one of the following interfaces for each multi-PHY
    - USB3.0 DRD
    - PCIe2.1
  - USB 3.0 Dual-Role Device (DRD) Controller
    - Static USB3.0 Device
    - Static USB3.0 xHCI host
  - PCIe2.1 interface
    - Compatible with PCI Express Base Specification Revision 2.1
    - Support one lane
    - Support dual operation mode:Root Complex (RC) and End Point (EP)
    - Support 2.5Gbps and 5.0Gbps serial data transmission rate per lane per direction

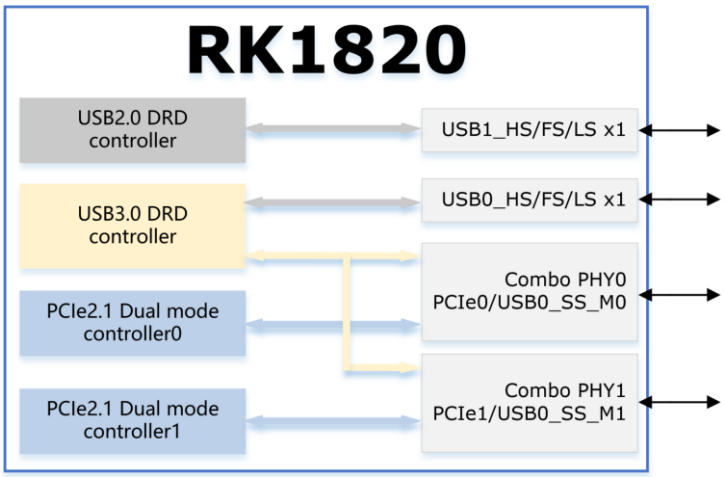

Fig. 1-1 RK1820 USB/PCIe controllers multiplexing relationship

- SPI interface
  - Support 2 SPI Controllers
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- I2C Master controller
  - Support 4 I2C ports in Master mode
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400K bits/s in the Fast-mode and up to 1M bit/s in high-speed mode

- SMBus slave interface
  - Support 1 independent SMBus
  - Supports slave mode of SMBus bus
  - Support SMBus protocol: write byte/read byte/read word/read 32 protocol/write 32 protocol/block write/block read
  - Support PEC
  - Support Alert
  - Support directed get UDID command
  - Clock stretching and wait state generation

- UART interface
  - Support 3 UART ports
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART2
  - Support RS485 function for UART2

- PWM
  - Support 3 channels
  - Support input capture mode
  - Support continuous mode and one-shot output mode
  - Support two-stage frequency division of working clock
  - Support power key capture mode
  - Support clock frequency meter
  - Support clock counter
- SAI
  - Support 1 SAI interfaces

- Support 4 TX lanes and 4 RX lanes
- Support audio protocol: I2S, PCM, TDM
- Support up to 128 slots available with configurable size
- Support slot length 8 to 32 bits configurable
- Support slot valid data length 8 to 32 bits configurable

1.2.8 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (a weak pull-up and a weak pull-down)
  - Support configurable drive strength

- Successive approximation ADC (SARADC)
  - Support 7 channels(One of them is only used for boot mode selection)
  - 13-bit resolution
  - Up to 2MS/s sampling rate
  - Support single mode and series conversion mode

- OTP
  - Support 8K bits size, 6.5K bits for secure application
  - Support Program/Read/Idle mode

1.3 RK1820 SODIMM Module Diagram

The following figure shows the basic block diagram.

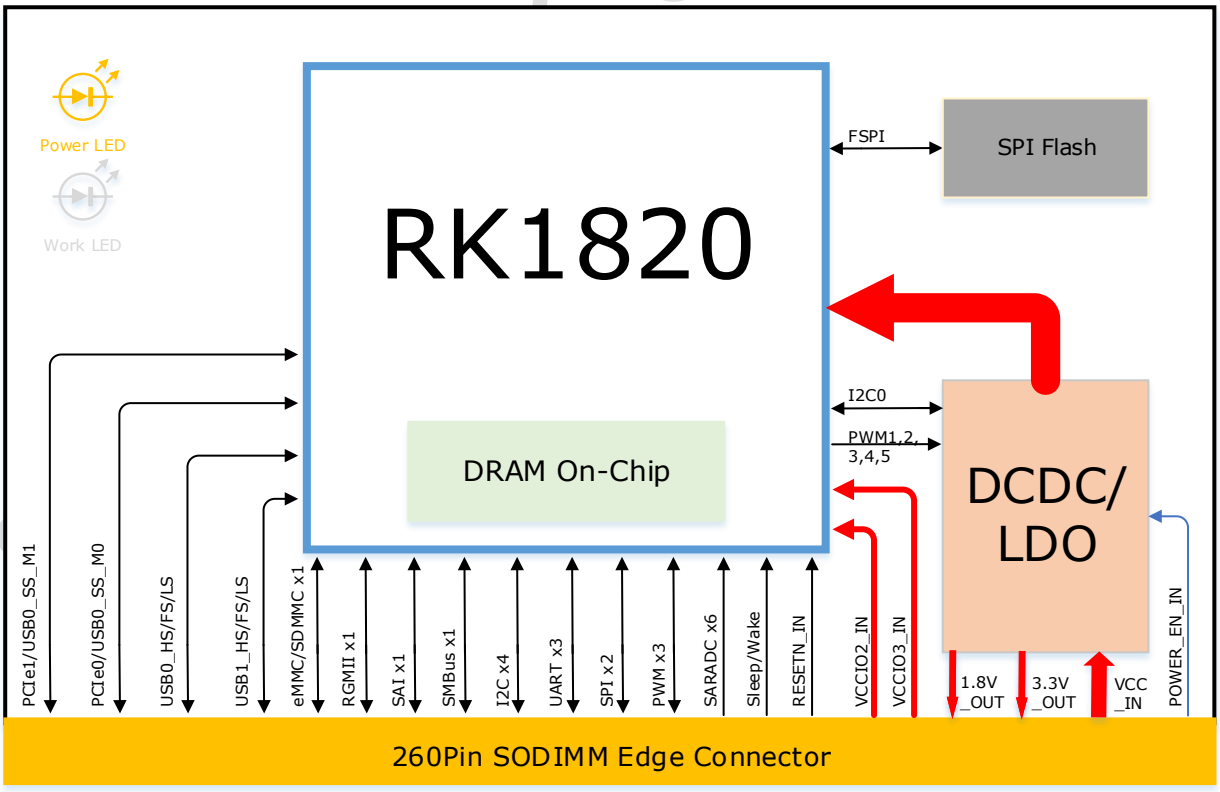

Fig. 1-2 RK1820 SODIMM Module Block Diagram

1.4 RK1820 SODIMM Module Typical Application

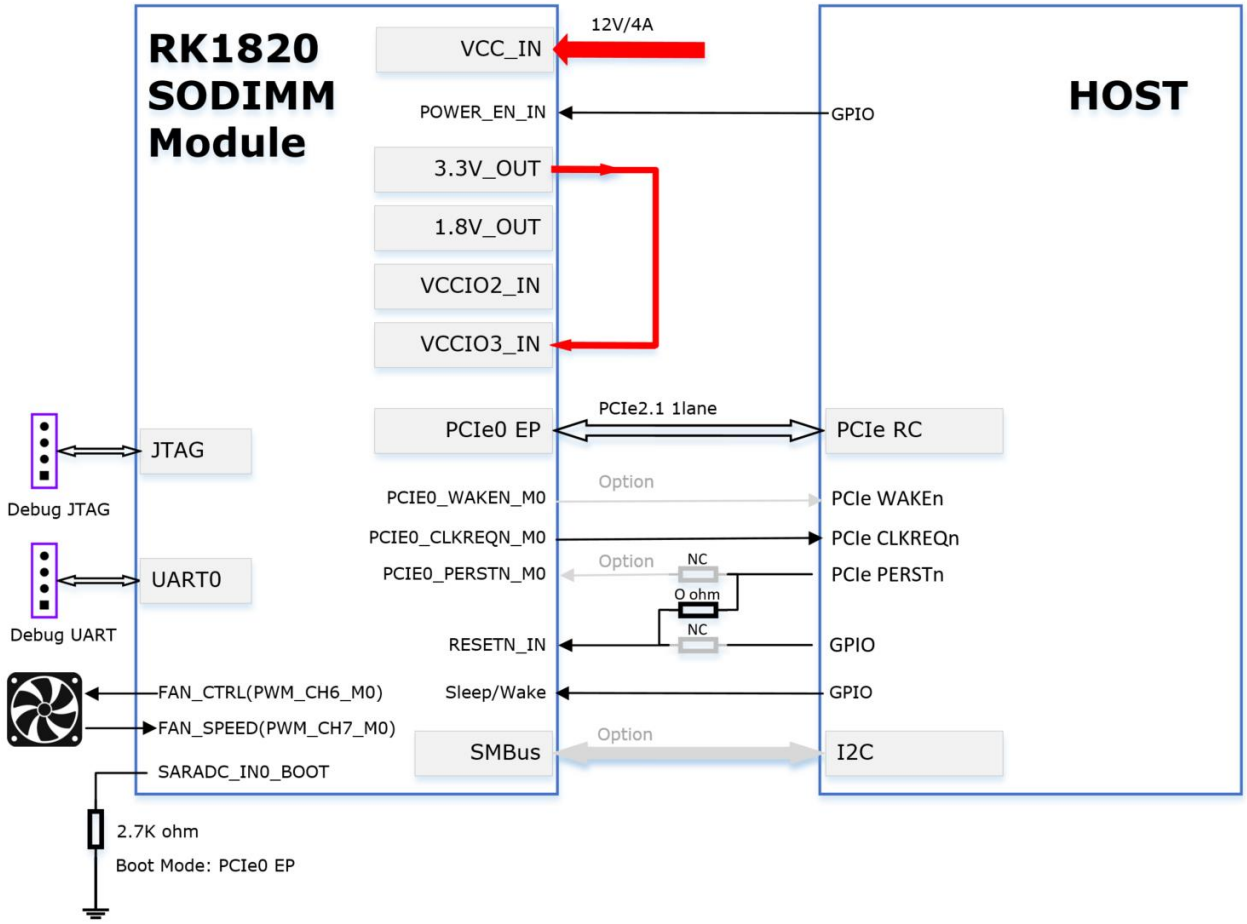

Fig. 1-3 RK1820 SODIMM Module PCIe interface Typical Application Block Diagram

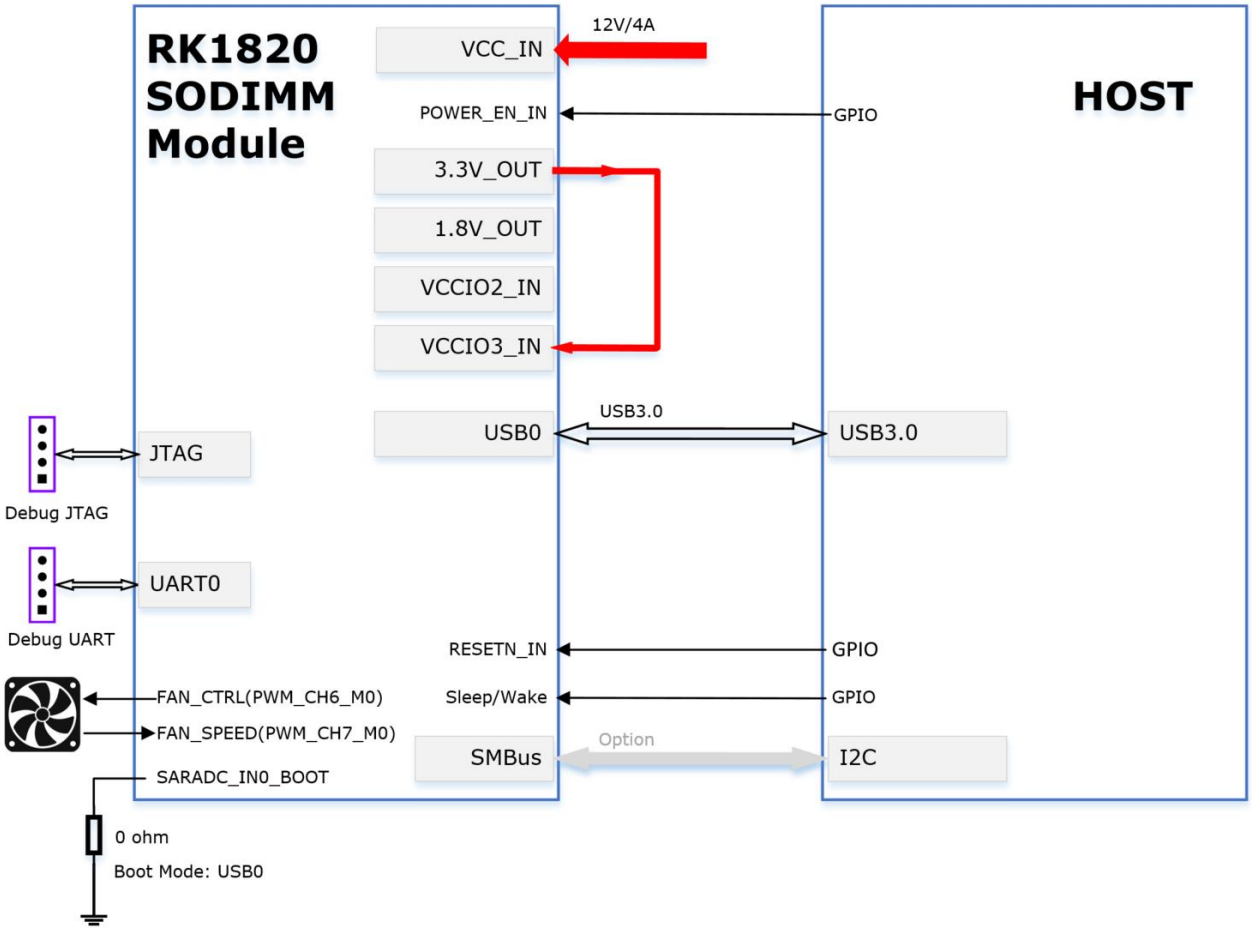

Fig. 1-4 RK1820 SODIMM Module USB3.0 interfacet Typical Application Block Diagram

Chapter 2 Module Information

2.1 Module Size

- 69.6mm x 45mm

2.2 External Connector

- The Module exposes a 260-pin SODIMM connector.
- Pin pitch:0.5mm.

2.3 Module Dimension

Note: All dimensions given in millimeter units.

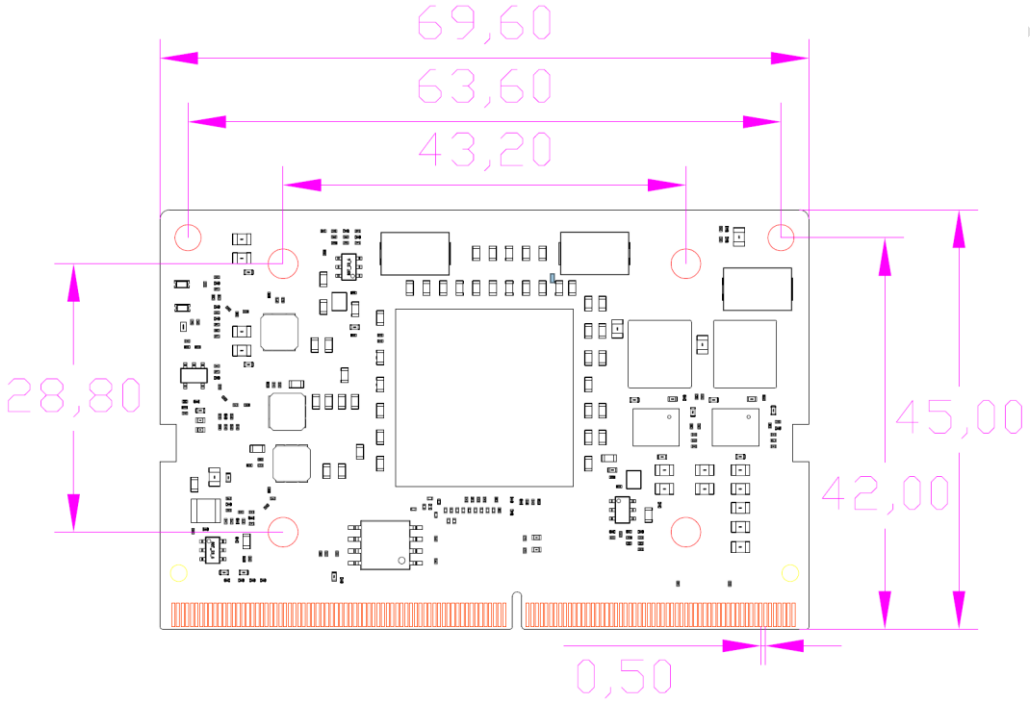

Fig. 2-1 RK1820 SODIMM Module without Heat sink Top View

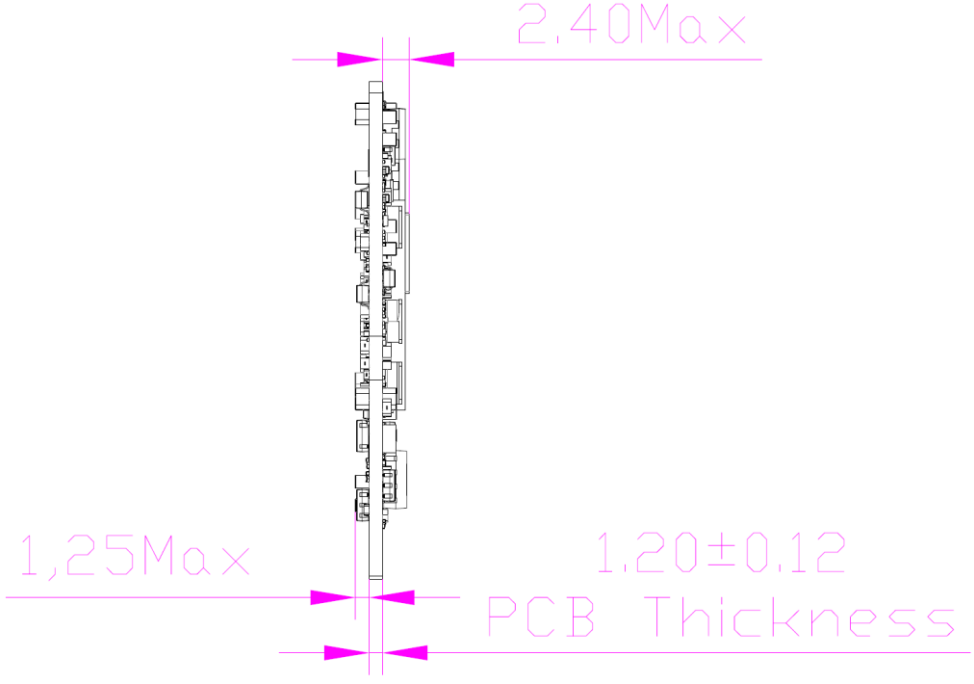

Fig. 2-2 RK1820 SODIMM Module without Heat sink Side View

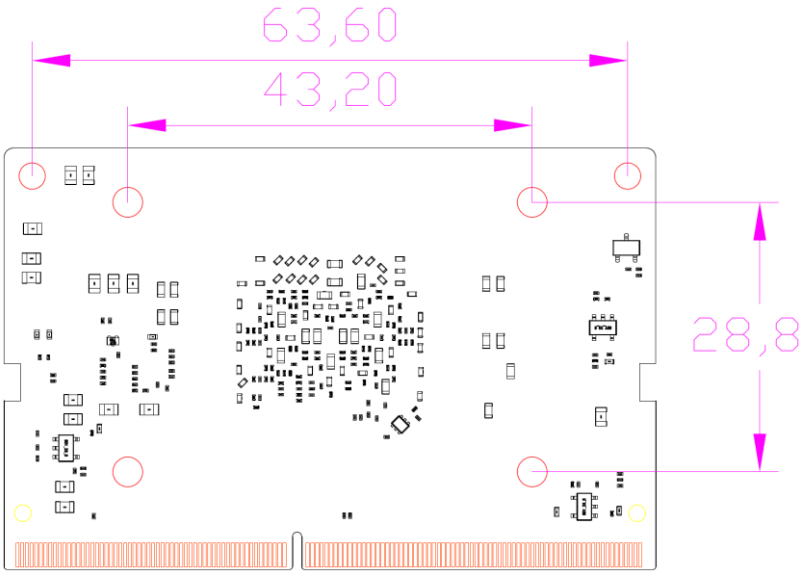

Fig. 2-3 RK1820 SODIMM Module without Heat sink Bottom View

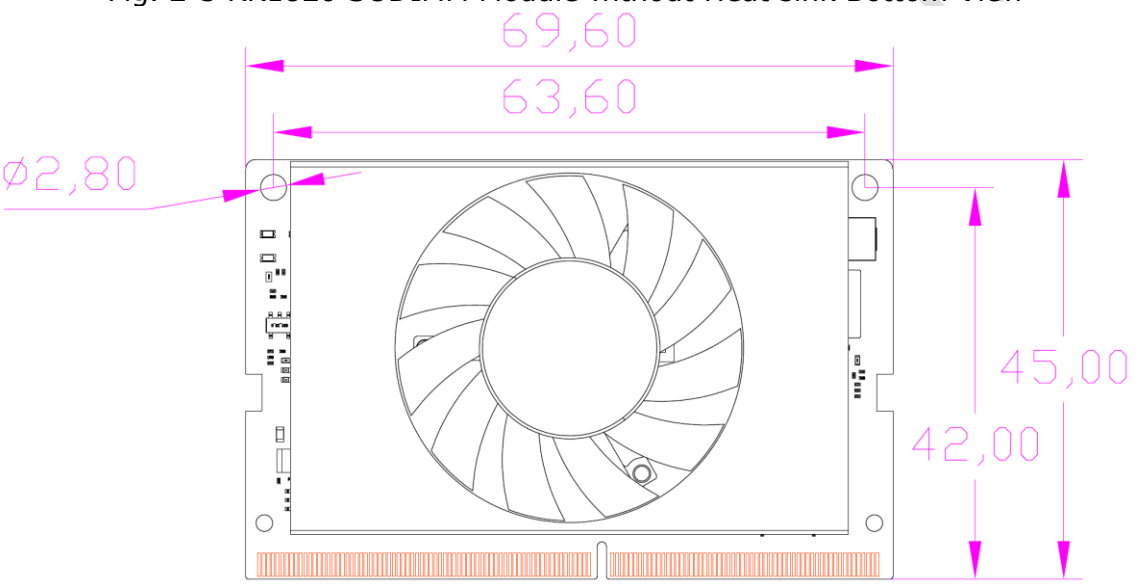

Fig. 2-4 RK1820 SODIMM Module with Heat sink Top View

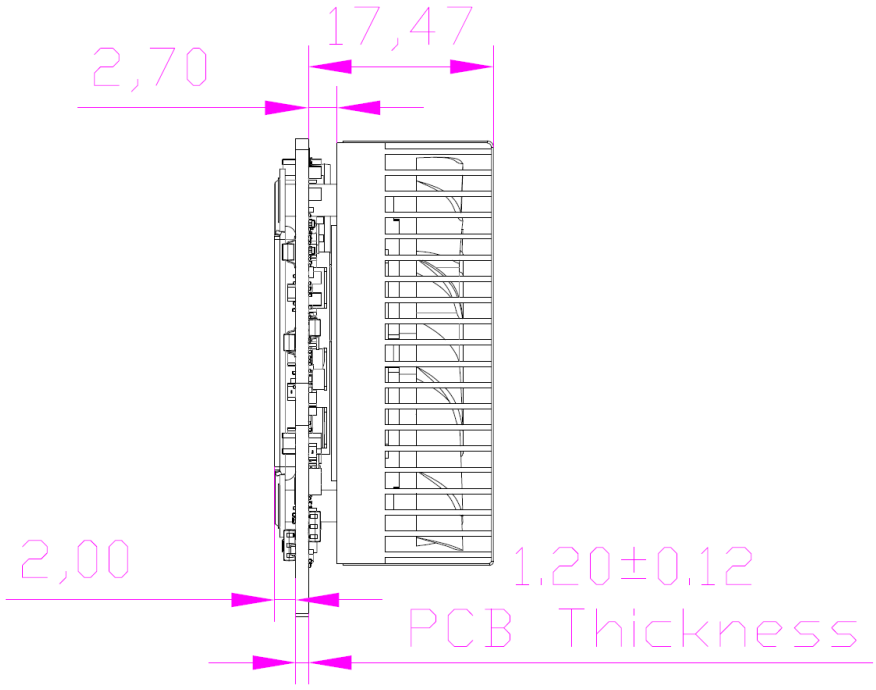

Fig. 2-5 RK1820 SODIMM Module with Heat sink Side View

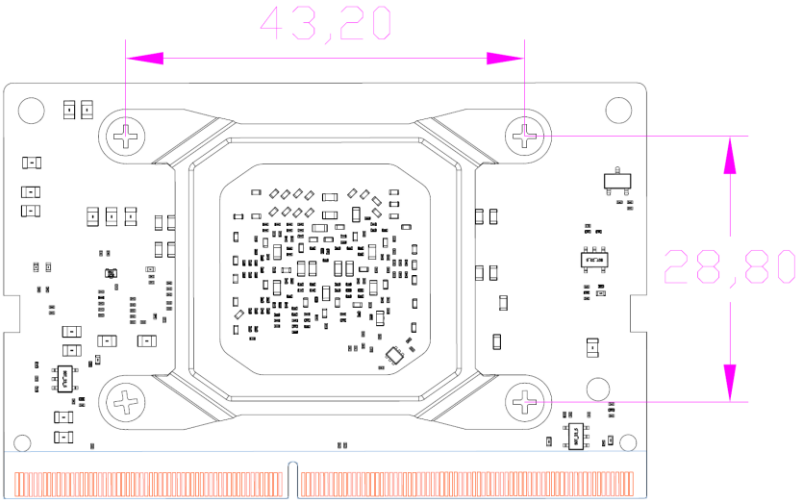

Fig. 2-6 RK1820 SODIMM Module with Heat sink Bottom View

2.4 Module Connector Pin Number List

Table 2-1 RK1820 SODIMM Module Pin Number Order Information

Pin Name	Pin #		Pin #	Pin Name
GND	1		2	GND
RSVD	3		4	RSVD
RSVD	5		6	RSVD
GND	7		8	GND
RSVD	9		10	RSVD
RSVD	11		12	RSVD
GND	13		14	GND
RSVD	15		16	RSVD
RSVD	17		18	RSVD
GND	19		20	GND
3.3V OUT	21		22	RSVD
3.3V OUT	23		24	RSVD
GND	25		26	GND
1.8V OUT	27		28	RSVD
1.8V OUT	29		30	RSVD
GND	31		32	GND
VCCIO2_IN	33		34	RSVD
VCCIO3_IN	35		36	RSVD
GND	37		38	GND
RSVD	39		40	RSVD
RSVD	41		42	RSVD
GND	43		44	GND
RSVD	45		46	RSVD
RSVD	47		48	RSVD
GND	49		50	GND
RSVD	51		52	RSVD
RSVD	53		54	RSVD
GND	55		56	GND
RSVD	57		58	RSVD
RSVD	59		60	RSVD
GND	61		62	GND
RSVD	63		64	RSVD
RSVD	65		66	RSVD
GND	67		68	GND
RSVD	69		70	RSVD
RSVD	71		72	RSVD
GND	73		74	GND
RSVD	75		76	RSVD
RSVD	77		78	RSVD
GND	79		80	GND
RSVD	81		82	RSVD
RSVD	83		84	RSVD
GND	85		86	GND
USB0_DRD_VBUSDET	87		88	RSVD
ETH_TXD0/PCIE1_WAKEN_M2/PWM_CH0_M1/SPI0_MOSI_M2/GPIO1_A6_d	89		90	RSVD
ETH_TXCTL/PCIE1_CLKREQN_M2/SPI0_CLK_M2/GPIO1_B2_d	91		92	RSVD
ETH_TXD1/PCIE1_PERSTN_M2/SPI0_MISO_M2/GPIO1_A7_d	93		94	RSVD
ETH_RXD0/SPI0_CS0N_M2/GPIO1_B4_d	95		96	RSVD
ETH_RXD1/SPI0_CS1N_M2/GPIO1_B5_d	97		98	RSVD

SARADC_IN6/PCIE0_PERSTN_M1/I2C4_SCL_M0/SAI_SDI2_M2/UART2_TX_M0/PWM_CH6_M2/GPIO1_D6_d	99		100	RSVD
SARADC_IN7/PCIE0_WAKEN_M1/I2C4_SDA_M0/SAI_SDI3_M2/UART2_RX_M0/PWM_CH7_M2/GPIO1_D7_d	101		102	GND
RSVD	103		104	ETH_TXD2/SPI1_MOSI_M2/GPIO1_B0_d
RSVD	105		106	ETH_TXCLK/I2C1_SCL_M1/SPI1_CLK_M2/GPIO1_B3_d
GND	107		108	ETH_TXD3/SPI1_MISO_M2/GPIO1_B1_d
USB0_DRD_DM	109		110	ETH_RXD2/I2C1_SDA_M1/SPI1_CS0N_M2/GPIO1_B6_d
USB0_DRD_DP	111		112	ETH_RXD3/I2C4_SCL_M1/SPI1_CS1N_M2/GPIO1_B7_d
GND	113		114	RSVD
USB1_DRD_DM	115		116	RSVD
USB1_DRD_DP	117		118	SARADC_IN5/PCIE0_CLKREQN_M1/SAI_SDI1_M2/SPI0_CS1N_M1/GPIO1_D5_d
GND	119		120	RSVD
RSVD	121		122	RSVD
RSVD	123		124	ETH_RXCTL/PCIE0_WAKEN_M2/GPIO1_C0_d
GND	125		126	ETH_RXCLK/I2C4_SDA_M1/GPIO1_C1_d
USB0_DRD_ID	127		128	ETH_MDC/PCIE0_PERSTN_M2/GPIO1_C2_d
GND	129		130	ETH_MDIO/PCIE0_CLKREQN_M2/GPIO1_C3_d
PCIE0_RXN/USB0_DRD_SSRXN_M0	131		132	GND
PCIE0_RXP/USB0_DRD_SSRXP_M0	133		134	PCIE0_TXN/USB0_DRD_SSTXN_M0
GND	135		136	PCIE0_TXP/USB0_DRD_SSTXP_M0
RSVD	137		138	GND
RSVD	139		140	RSVD
GND	141		142	RSVD
RSVD	143		144	GND
RSVD	145		146	GND
GND	147		148	RSVD
RSVD	149		150	RSVD
RSVD	151		152	GND
GND	153		154	RSVD
RSVD	155		156	RSVD
RSVD	157		158	GND
GND	159		160	PCIE0_REFCLKN
PCIE1_RXN/USB0_DRD_SSRXN_M1	161		162	PCIE0_REFCLKP
PCIE1_RXP/USB0_DRD_SSRXP_M1	163		164	GND
GND	165		166	PCIE1_TXN/USB0_DRD_SSTXN_M1
RSVD	167		168	PCIE1_TXP/USB0_DRD_SSTXP_M1
RSVD	169		170	GND
GND	171		172	RSVD
PCIE1_REFCLKN	173		174	RSVD
PCIE1_REFCLKP	175		176	GND
GND	177		178	RSVD
I2C2_SCL_M0/UART1_CTSN_M0/PCIE0_WAKEN_M0/SMBUS_ALERT_M0/SAI_SDI0_M0/SAI_SDO3_M0/GPIO0_B5_d	179		180	PCIE0_CLKREQN_M0/SAI_LRCK_M0/GPIO0_B7_d
I2C2_SDA_M0/UART1_RTSN_M0/PCIE0_PERSTN_M0/SAI_SCLK_M0/GPIO0_B6_d	181		182	RSVD
RSVD	183		184	RSVD
ETH_CLK_25M_OUT/I2C2_SCL_M1/SAI_SDO2_M2/UART2_CTSN_M0/SPI1_CS1N_M1/GPIO1_C4_d	185		186	RSVD
ETH_MCLK/I2C2_SDA_M1/SAI_SDO1_M2/UART2_RTSN_M0/PWM_CH0_M2/SPI1_MOSI_M1/GPIO1_C5_d	187		188	RSVD
SARADC_IN2/SMBUS_SCL_M1/I2C3_SCL_M1/SAI_SDO3_M2/UART1_TX_M1/PWM_CH6_M1/SPI0_MOSI_M1/GPIO1_D2_d	189		190	RSVD
SARADC_IN3/SMBUS_SDA_M1/I2C3_SDA_M1/UART1_RX_M1/PWM_CH7_M1/SPI0_MISO_M1/GPIO1_D3_d	191		192	RSVD
SARADC_IN4/SMBUS_ALERT_M1/SAI_SDO0_M2/UART1_CTSN_M1/SPI0_CS0N_M1/GPIO1_D4_d	193		194	RSVD
PCIE1_CLKREQN_M0/SAI_SDI0_M2/UART1_RTSN_M1//SPI0_CLK_M1/GPIO1_D1_d	195		196	RSVD
ETH_PPSTRIG/PCIE1_PERSTN_M0/SAI_LRCK_M2/SPI1_CLK_M1/GPIO1_D0_d	197		198	RSVD
ETH_PPSCLK/PCIE1_WAKEN_M0/SAI_SCLK_M2/SPI1_CS0N_M1/GPIO1_C7_d	199		200	GND
GND	201		202	RSVD
JTAG_TCK_M0/UART1_TX_M0_d	203		204	RSVD
JTAG_TMS_M0/UART1_RX_M0_d	205		206	I2C3_SCL_M0/PWM_CH6_M0/SPI1_CLK_M0/SMBUS_SCL_M0/SAI_SDI2_M0/SAI_SDO1_M0/GPIO0_B3_d
RSVD	207		208	I2C3_SDA_M0/PWM_CH7_M0/SPI1_MOSI_M0/SMBUS_SDA_M0/SAI_SDI1_M0/SAI_SDO2_M0/GPIO0_B4_d
RSVD	209		210	RSVD
ETH_PTP_REFCLK/SAI_MCLK_M2/SPI1_MISO_M1/GPIO1_C6_d	211		212	RSVD
RSVD	213		214	SARADC_IN0_BOOT
RSVD	215		216	RSVD
NC(MODULE_ID)	217		218	PWR_CTRL1/PWM_CH0_M0/SPI1_CS1N_M0/GPIO0_A3_d
SDMMC_D0/SAI_SDO2_M1/UART1_CTSN_M2/GPIO0_D2_u	219		220	SDMMC_D7/I2C2_SDA_M2/SAI_SDO0_M1/UART2_RTSN_M2/PCIE1_WAKEN_M1/GPIO1_A1_u
SDMMC_D1/SAI_SDO3_M1/UART1_RTSN_M2/GPIO0_D3_u	221		222	SDMMC_D6/I2C2_SCL_M2/SAI_SDI0_M1/UART2_CTSN_M2/SMBUS_ALERT_M2/GPIO1_A0_u

SDMMC_D2/SAI_SDI2_M1/UART1_TX_M2/GPIO0_D4_u	223		224	SDMMC_D5/I2C4_SDA_M2/SAI_LRCK_M1/UART2_RX_M2/SMBUS_SDA_M2/GPIO0_D7_u
SDMMC_D3/SAI_SDI3_M1/UART1_RX_M2/GPIO0_D5_u	225		226	SDMMC_D4/I2C4_SCL_M2/SAI_SCLK_M1/UART2_TX_M2/SMBUS_SCL_M2/GPIO0_D6_u
SDMMC_CMD/GPIO1_A2_u	227		228	RSVD
SDMMC_CLK_OUT/SAI_SDO1_M1/GPIO1_A3_d	229		230	RSVD
GND	231		232	SDMMC_RSTN/I2C3_SCL_M2/SAI_SDI1_M1/PCIE1_PERSTN_M1/GPIO1_A4_u
RSVD	233		234	SDMMC_DETN/I2C3_SDA_M2/SAI_MCLK_M1/PCIE1_CLKREQN_M1/GPIO1_A5_u
RSVD	235		236	JTAG_TCK_M1/UART0_TX_u
POWER_EN_IN	237		238	JTAG_TMS_M1/UART0_RX_u
RESETN_IN_u	239		240	Sleep/Wake(GPIO0_A0)_d
GND	241		242	GND
GND	243		244	GND
GND	245		246	GND
GND	247		248	GND
GND	249		250	GND
VCC_IN	251		252	VCC_IN
VCC_IN	253		254	VCC_IN
VCC_IN	255		256	VCC_IN
VCC_IN	257		258	VCC_IN
VCC_IN	259		260	VCC_IN

2.5 Pin Function description

See the RK1820 SODIMM Module Pinout for details on connecting to each of the interfaces.

Table 2-2 Power and System Control Pin Descriptions

Pin#	Signal Name	Description	Direction	Pin Type
251 252 253 254 255 256 257 258 259 260	VCC_IN	Main power: Supply provides power to the module.	Input	8V to 14.4V
237	POWER_EN_IN	Signal for Module ON/OFF: High level on, Low level off. A 100kΩ pulldown is also on the module.	Input	1.5V to VCC_IN
21 23	3.3V_OUT	The power output on the module is only provided to the VCCIO2 or VCCIO3 power domain and related external devices.	Output	3.3V
27 29	1.8V_OUT	The power output on the module is only provided to the VCCIO2 or VCCIO3 power domain and related external devices.	Output	1.8V
33	VCCIO2_IN	VCCIO2 domain power supply.	Input	1.8V/3.3V
35	VCCIO3_IN	VCCIO3 domain power supply.	Input	1.8V/3.3V
240	Sleep/Wake	Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	Input	3.3V Domain
239	RESETN_IN	Module Reset. Reset to the module when driven low by HOST. 1kΩ pull-up to 3.3V on the module.	Input	3.3V Domain
214	SARADC_IN0_BOOT	BOOT mode configuration. 10kΩ pull-up to 1.8V on the module.	Input	1.8V Domain
217	MODULE_ID	Reserved, this module is not used	NA	NA

Table 2-3 USB/PCIe Pin Descriptions

Pin#	Signal Name	Description	Direction	Pin Type
136	PCIE0_TXP/USB0_DRD_SSTXP_M0	PCIe0 transmit differential Positive USB0 DRD SuperSpeed transmit differential Positive(Mux0)	Output	Combo PHY
134	PCIE0_TXN/USB0_DRD_SSTXN_M0	PCIe0 transmit differential Negative USB0 DRD SuperSpeed transmit differential Negative(Mux0)	Output	Combo PHY
133	PCIE0_RXP/USB0_DRD_SSRXP_M0	PCIe0 receive differential Positive USB0 DRD SuperSpeed receive differential Positive(Mux0)	Input	Combo PHY
131	PCIE0_RXN/USB0_DRD_SSRXN_M0	PCIe0 receive differential Negative USB0 DRD SuperSpeed receive differential Negative(Mux0)	Input	Combo PHY
162	PCIE0_REFCLKP	PCIe0 differential clock Positive,Support input or output	Bidir	Combo PHY
160	PCIE0_REFCLKN	PCIe0 differential clock Negative,Support input or output	Bidir	Combo PHY
168	PCIE1_TXP/USB0_DR	PCIe1 transmit differential Positive	Output	Combo PHY

	D_SSTXP_M1	USB0 DRD SuperSpeed transmit differential Positive(Mux1)		
166	PCIE1_TXN/USB0_DRD_SSTXN_M1	PCIe1 transmit differential Negative USB0 DRD SuperSpeed transmit differential Negative(Mux1)	Output	Combo PHY
163	PCIE1_RXP/USB0_DRD_SSRXP_M1	PCIe1 receive differential Positive USB0 DRD SuperSpeed receive differential Positive(Mux1)	Input	Combo PHY
161	PCIE1_RXN/USB0_DRD_SSRXN_M1	PCIe1 receive differential Negative USB0 DRD SuperSpeed receive differential Negative(Mux1)	Input	Combo PHY
175	PCIE1_REFCLKP	PCIe1 differential clock Positive,Support input or output	Bidir	Combo PHY
173	PCIE1_REFCLKN	PCIe1 differential clock Negative,Support input or output	Bidir	Combo PHY
111	USB0_DRD_DP	USB0 DRD HS/FS/LS Data Plus	Bidir	USB PHY
109	USB0_DRD_DM	USB0 DRD HS/FS/LS Data Minus	Bidir	USB PHY
127	USB0_DRD_ID	USB0 DRD ID detect	Input	1.8V Domain
87	USB0_DRD_VBUSDET	USB0 DRD connected vbus power detect	Input	3.3V Domain
117	USB1_DRD_DP	USB1 DRD HS/FS/LS Data Plus	Bidir	USB PHY
115	USB1_DRD_DM	USB1 DRD HS/FS/LS Data Minus	Bidir	USB PHY

Table 2-4 GPIO Power Domain Descriptions

Pin#	Signal Name	Power Domain
218	PWR_CTRL1/PWM_CH0_M0/SPI1_CS1N_M0/GPIO0_A3_d	Operating Voltage:3.3V
206	I2C3_SCL_M0/PWM_CH6_M0/SPI1_CLK_M0/SMBUS_SCL_M0/SAI_SDI2_M0/SAI_SDO1_M0/GPIO0_B3_d	
208	I2C3_SDA_M0/PWM_CH7_M0/SPI1_MOSI_M0/SMBUS_SDA_M0/SAI_SDI1_M0/SAI_SDO2_M0/GPIO0_B4_d	
179	I2C2_SCL_M0/UART1_CTSN_M0/PCIE0_WAKEN_M0/SMBUS_ALERT_M0/SAI_SDI0_M0/SAI_SDO3_M0/GPIO0_B5_d	
181	I2C2_SDA_M0/UART1_RTSN_M0/PCIE0_PERSTN_M0/SAI_SCLK_M0/GPIO0_B6_d	
180	PCIE0_CLKREQN_M0/SAI_LRCK_M0/GPIO0_B7_d	
203	JTAG_TCK_M0/UART1_TX_M0_d	
205	JTAG_TMS_M0/UART1_RX_M0_d	
236	JTAG_TCK_M1/UART0_TX_u	
238	JTAG_TMS_M1/UART0_RX_u	
219	SDMMC_D0/SAI_SDO2_M1/UART1_CTSN_M2/GPIO0_D2_u	VCCIO2 Domain Operating Voltage:1.8V or 3.3V
221	SDMMC_D1/SAI_SDO3_M1/UART1_RTSN_M2/GPIO0_D3_u	
223	SDMMC_D2/SAI_SDI2_M1/UART1_TX_M2/GPIO0_D4_u	
225	SDMMC_D3/SAI_SDI3_M1/UART1_RX_M2/GPIO0_D5_u	
226	SDMMC_D4/I2C4_SCL_M2/SAI_SCLK_M1/UART2_TX_M2/SMBUS_SCL_M2/GPIO0_D6_u	
224	SDMMC_D5/I2C4_SDA_M2/SAI_LRCK_M1/UART2_RX_M2/SMBUS_SDA_M2/GPIO0_D7_u	
222	SDMMC_D6/I2C2_SCL_M2/SAI_SDI0_M1/UART2_CTSN_M2/SMBUS_ALERT_M2/GPIO1_A0_u	
220	SDMMC_D7/I2C2_SDA_M2/SAI_SDO0_M1/UART2_RTSN_M2/PCIE1_WAKEN_M1/GPIO1_A1_u	
227	SDMMC_CMD/GPIO1_A2_u	
229	SDMMC_CLK_OUT/SAI_SDO1_M1/GPIO1_A3_d	
232	SDMMC_RSTN/I2C3_SCL_M2/SAI_SDI1_M1/PCIE1_PERSTN_M1/GPIO1_A4_u	
234	SDMMC_DETN/I2C3_SDA_M2/SAI_MCLK_M1/PCIE1_CLKREQN_M1/GPIO1_A5_u	
89	ETH_TXD0/PCIE1_WAKEN_M2/PWM_CH0_M1/SPI0_MOSI_M2/GPIO1_A6_d	VCCIO3 Domain Operating Voltage:1.8V or 3.3V
93	ETH_TXD1/PCIE1_PERSTN_M2/SPI0_MISO_M2/GPIO1_A7_d	
104	ETH_TXD2/SPI1_MOSI_M2/GPIO1_B0_d	
108	ETH_TXD3/SPI1_MISO_M2/GPIO1_B1_d	
91	ETH_TXCTL/PCIE1_CLKREQN_M2/SPI0_CLK_M2/GPIO1_B2_d	
106	ETH_TXCLK/I2C1_SCL_M1/SPI1_CLK_M2/GPIO1_B3_d	
95	ETH_RXD0/SPI0_CS0N_M2/GPIO1_B4_d	
97	ETH_RXD1/SPI0_CS1N_M2/GPIO1_B5_d	
110	ETH_RXD2/I2C1_SDA_M1/SPI1_CS0N_M2/GPIO1_B6_d	
112	ETH_RXD3/I2C4_SCL_M1/SPI1_CS1N_M2/GPIO1_B7_d	
124	ETH_RXCTL/PCIE0_WAKEN_M2/GPIO1_C0_d	
126	ETH_RXCLK/I2C4_SDA_M1/GPIO1_C1_d	
128	ETH_MDC/PCIE0_PERSTN_M2/GPIO1_C2_d	
130	ETH_MDIO/PCIE0_CLKREQN_M2/GPIO1_C3_d	
185	ETH_CLK_25M_OUT/I2C2_SCL_M1/SAI_SDO2_M2/UART2_CTSN_M0/SPI1_CS1N_M1/GPIO1_C4_d	
187	ETH_MCLK/I2C2_SDA_M1/SAI_SDO1_M2/UART2_RTSN_M0/PWM_CH0_M2/SPI1_MOSI_M1/GPIO1_C5_d	
211	ETH_PTP_REFCLK/SAI_MCLK_M2/SPI1_MISO_M1/GPIO1_C6_d	
199	ETH_PPSCLK/PCIE1_WAKEN_M0/SAI_SCLK_M2/SPI1_CS0N_M1/GPIO1_C7_d	
197	ETH_PPSTRIG/PCIE1_PERSTN_M0/SAI_LRCK_M2/SPI1_CLK_M1/GPIO1_D0_d	
195	PCIE1_CLKREQN_M0/SAI_SDI0_M2/UART1_RTSN_M1//SPI0_CLK_M1/GPIO1_D1_d	
189	SARADC_IN2/SMBUS_SCL_M1/I2C3_SCL_M1/SAI_SDO3_M2/UART1_TX_M1/PWM_CH6_M1/SPI0_MOSI_M1/GPIO1_D2_d	
191	SARADC_IN3/SMBUS_SDA_M1/I2C3_SDA_M1/UART1_RX_M1/PWM_CH7_M1/SPI0	

	_MISO_M1/GPIO1_D3_d	
193	SARADC_IN4/SMBUS_ALERT_M1/SAI_SDO0_M2/UART1_CTSN_M1/SPI0_CS0N_M1/GPIO1_D4_d	
118	SARADC_IN5/PCIE0_CLKREQN_M1/SAI_SDI1_M2/SPI0_CS1N_M1/GPIO1_D5_d	
99	SARADC_IN6/PCIE0_PERSTN_M1/I2C4_SCL_M0/SAI_SDI2_M2/UART2_TX_M0/PWM_CH6_M2/GPIO1_D6_d	
101	SARADC_IN7/PCIE0_WAKEN_M1/I2C4_SDA_M0/SAI_SDI3_M2/UART2_RX_M0/PWM_CH7_M2/GPIO1_D7_d	

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for VCC_IN	VCC_IN	-0.3	18	V
1.8V/3.3V supply voltage for VCCIO	VCCIO2_IN VCCIO3_IN	-0.3	3.8	V
Max Conjunction Temperature	Tj	NA	105	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Related Power Group	Min	Typ	Max	Unit	Note
Supply voltage for VCC_IN	VCC_IN	8.0	12.0	14.4	V	1
Supply current for VCC_IN	I_{VCC_IN}	4.0	-	5.0	A	
Output power supply peak current for 3.3V_OUT	$I_{3.3V\_OUT}$	-	-	0.8	A	2
Output power supply peak current for 1.8V_OUT	$I_{1.8V\_OUT}$	-	-	0.3	A	
1.8V/3.3V supply voltage for VCCIO	VCCIO2_IN VCCIO3_IN	1.62 2.97	1.8 3.3	1.98 3.63	V	
Storage Temperature	Tstg	-20	-	70	℃	
Storage relative humidity		30	-	70	%	3
Ambient Operating Temperature	Ta	TBD	25	TBD	℃	4
Max Conjunction Temperature	Tj	-	-	95	℃	

Notes:
1. Considering the maximum contact current rating of each contact of SODIMM Socket (generally 0.5A), it is recommended that the power supply voltage is 12V. When the power supply capacity can provide more than 40W, each pin should not exceed 0.5A.
   The power consumption corresponding to different performance modes，see RK1820 SODIMM Module Thermal Design Guide for details.
2. By default, it is only used for VCCIO2/VCCIO3 power domain.If external devices also want to use it, the VCC_IN input power should be increased accordingly.
3. No condensation
4. Customers should consider specific thermal design for the final product based on the specific environment, performance requirements and operational conditions.

3.3 Electrical Characteristics for Output power

Table 3-3 Electrical Characteristics for Output power

Parameters	Related Power Group	Min	Typ	Max	Unit
Vout Accuracy	3.3V_OUT	-3	-	3	%
Vout Accuracy	1.8V_OUT	-3	-	3	%

3.4 DC Characteristics for GPIO

Table 3-4 DC Characteristics for GPIO

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VCCIO+0.3	V

Parameters		Symbol	Min	Typ	Max	Unit
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VCCIO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VCCIO	V
	Input High Voltage	Vih	0.65*VCCIO	NA	VCCIO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VCCIO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm

3.5 Electrical Characteristics for USB2.0 Interface

Table 3-5 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.6 Electrical Characteristics for SARADC

Table 3-6 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution	ENOB	f_S=1MS/s fclk=24MHz	NA	11.2	13	bit
Analog Input Channel			NA	NA	8	
Analog Input Range	VIN		0	NA	1.8	V
Analog Input maximum voltage					3.3	V
Differential Non-Linearity	DNL		NA	±1	±3	LSB
Integral Non-Linearity	INL		NA	±2	±6	LSB
Conversion Rage	f_S		NA	1	NA	MS/s
Signal to Noise and Distortion Ratio	SINAD	f_S=1MS/s f_{OUT}=1.17KHz	NA	69.2	NA	dB
Total Harmonic Distortion	THD		NA	77.3	NA	dB

3.7 Electrical Characteristics for Multi-PHY

Table 3-7 Electrical Characteristics for PCIe PHY

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Transmitter						
Differential p-pTx voltage swing	$V_{TX-DIFF-PP}$		0.8	NA	1.2	V
Low power differential p-p Tx voltage swing	$V_{TX-DIFF-PP-LOW}$		0.4	NA	1.2	V
Tx de-emphasis level ratio	$R_{TX-DIFF-DC}$		80	NA	120	ohm
Single Ended Output Resistance Matching	$R_{TX-DC-OFFSET}$		NA	NA	5	%
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		NA	NA	600	mV
Output rising time for 20% to 80%	Tr		25	NA	NA	ps
Output falling time for 20% to 80%	Tf		25	NA	NA	ps
AC Coupling Capacitor(USB3.0/PCIE)	C_{TX}		75	NA	200	nF
Unit Interval	UI		399.88	NA	400.12	ps
Input Voltage Swing	$V_{rxdpp-c}$		250	NA	1200	mV
Input differential impedance	R_{rxd-c}		80	NA	120	ohm
Single Ended input Resistance Matching	$T_{rxd-c-ms}$		NA	NA	5	%

Chapter 4 RK1820 Thermal Management

See the RK1820 SODIMM Module Thermal Design Guide for details.

