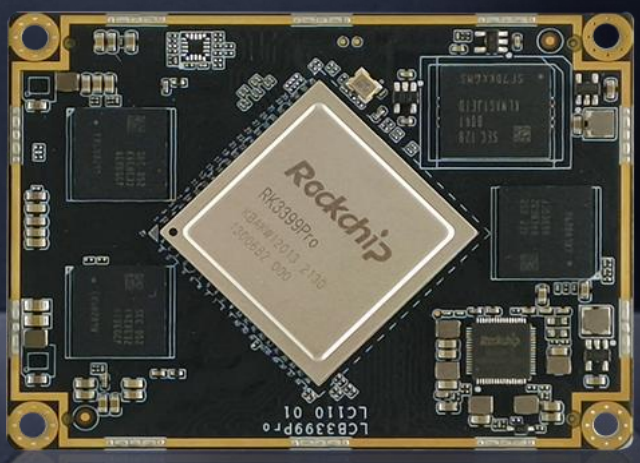
neardi

LCB3399Pro System On Module

Datasheet

V1.0



Shanghai Neardi Technology Co., Ltd.

www.neardi.com

Notes: All contengs only for explanatory and descriptive purposes. Please refer to the actual product. We strive to ensure consistency with the actual product. This document is provided for customers as a reference for product design and end application. It is better for you confirm the specifications and parameters carefully, provided in the document to ensure they meet the design or application requirements of the product. Whatsmore, it is strongly recommended that customers conduct detailed tests based on our actual products in the actual application scenario to ensure they meet the final usage requirements. Neardi Technology does not assume any responsibility for any damage suffered due to the use of the document, materials, and product functions.

Due to product version upgrades or other needs, our company may update the manual. If you need the latest version of the manual, please contact our company. We always adhere to the principle of customer first and provide customers with fast and efficient support services. If you have any needs, please feel free to contact our company at any time. Contact information is as follows:

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Version History

Version	Date	Description
V1.0	2022/8/23	Initial version

Contents

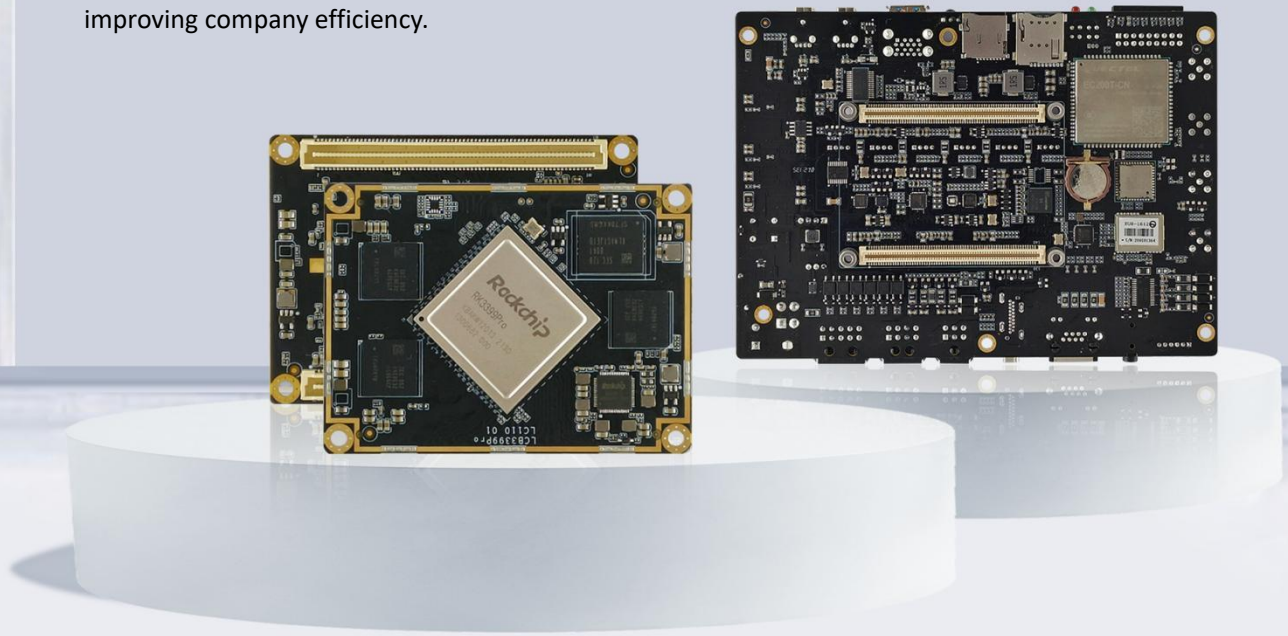
1.Product Introduction

The LCB3399Pro is a full-featured core module exquisitely designed based on the Rockchip RK3399Pro chip platform, with dimensions of only 75mm by 55mm. The connection between the core module and the baseboard uses two Tyco/AMP 0.8mm pitch dual-row 140Pin board-to-board connectors, secured with four M3 screws, ensuring stability, reliability, ease of installation, and maintenance.

The LCB3399Pro includes CPU (with integrated NPU), DDR, eMMC, and PMU components. The CPU is the RK3399 Pro; DDR uses the market mainstream LPDDR3, with dual-channel 64-bit bandwidth, lower power consumption, and higher frequency, available in 3GB/6GB configurations; eMMC adopts the high-speed eMMC 5.1 standard, with various capacity configurations from 4GB to 128GB; the PMU consists of the RK809 and multiple DC-DC and LDO components, with CPU core voltages supporting DVFS (Dynamic Voltage and Frequency Scaling).

The LCB3399Pro has undergone a rigorous testing process management to ensure long-term stable and reliable operation. It can provide customers with the following test data for reference: functional item testing, accuracy, ripple, overshoot, drop, rise time, and dynamic range testing of power supply voltage, power-up sequence testing of various voltages, accuracy and frequency deviation testing of key clock signals, power consumption testing under full load, and temperature rise testing under full load.

The LCB3399Pro adopts a modular design concept, designing the core part, which has the same requirements and strict standards, as a full-function module, and has undergone comprehensive testing and mass verification. Users can develop products based on this module, saving project development time, reducing corporate costs, and improving company efficiency.



2. Function Overview

High-Performance Processor

CPU	Dual-core Cortex-A72 and quad-core Cortex-A53 architecture, with a clock speed up to 1.8GHz, offering high performance and low power consumption.
GPU	ARM Mali-T860MP4 GPU, supporting AFBC (Advanced Frame Buffer Compression).
NPU	3 TOPS of computational power.
VPU	Capable of 4K/1080P video encoding and decoding, with 4K display output.
DDR	LPDDR4/4x, with options for 3GB or 6GB.
eMMC	eMMC 5.1, with options for 16GB or 64GB.

Operating System

Android

Linux （Buildroot / Debian / Ubuntu）

Open Source Materials

WIKI Documentation http://www.neardi.com/cms/en/wiki.html

Quick Start

Firmware Upgrade

Android Development

Linux Development

Kernel Drivers

DEMO

System Customization

Accessories

Frequently Asked Questions (FAQ)

Release Notes

Hardware Materials

Chip Datesheet

Product 2D/3D Drawings

Core Board Pin Definitions

Baseboard Reference Schematic

Baseboard Reference PCB

Key Bill of Materials (BOM)

Software Materials

Firmware Tools and Drivers

Android Source Code and Images

U-Boot and Kernel Source Code

Debian/Ubuntu/Buildroot System Files

3. Technical Specifications

Basic Parameters	
SOC	RK3399Pro; a dual-core Cortex-A72 plus quad-core Cortex-A53 architectural processor.
GPU	Mali-T860MP4 GPU, supporting OpenGL ES 1.1/2.0/3.0/3.1, OpenVG 1.1, OpenCL, DirectX 11; supports AFBC (Advanced Frame Buffer Compression).
NPU	3 TOPS computational power; supports 8-bit/16-bit operations; compatible with TensorFlow and Caffe models.
VPU	Capable of 4K VP9 and 4K 10-bit H265/H264 video decoding, up to 60fps at 1080P; multi-format video decoding (WMV, MPEG-1/2/4, VP8); 1080P video encoding, supporting H.264 and VP8 formats.
DDR	LPDDR4/LPDDR4X, with options for 3GB or 6GB.
eMMC	eMMC 5.1, with options for 16GB, 32GB, 64GB, or 128GB.
PMU	RK806
OS	Android / Ubuntu / Buildroot / Debian

Hardware Specifications	
Camera Interface	Two ISP built-in
	Dual MIPI-CSI 4 Lane of 1.5 Gbps/Lane
	ITU-R BT 601/656 compliant
	Maximum input resolution of one ISP is 14M pixels

Display Interface	Two VOP embedded
	Dual MIPI-DSI 4 Lane of 1.5 Gbps/Lane up to 2560x1600@60fps
	eDP1.3 4 Lane of 2.7/1.62 Gbps/lane
	DP1.2 4 Lane with HDCP2.2 up to 4kx2k at 60Hz resolution
	HDMI2.0 3 Lane with HDCP2.2
USB Interface	OTG*1，HOST*2，TYPE-C*2
TYPE-C Interface	Dual Type-C PHY with Type-C V1.1 and USB PD2.0
	Attach/detach detection and signaling as DFP, UFP and DRP
	Support USB3.0 Type-C and DisplayPort 1.2 Alt Mode
	Up to 5Gbps data rate for USB3.0
	Up to 5.4Gbps (HBR2) data rate for DP1.2
Audio Interface	Three I2S/PCM built-in
	SPDIF supported
	Audio resolution from 16bits to 32bits
	Sample rate up to 192KHz
	Provides master and slave work mode, software configurable
	Support 3 I2S formats (normal, left-justified, right-justified)
	Support 4 PCM formats (early, late1, late2, late3)
	Support two 16-bit audio data store together in one 32-bit wide location
	Support 16, 20, 24 bits audio data transfer in linear PCM mode
Connectivity	Compatible with SDIO 3.0 protocol
	GMAC 10/100/1000M Ethernet Controller

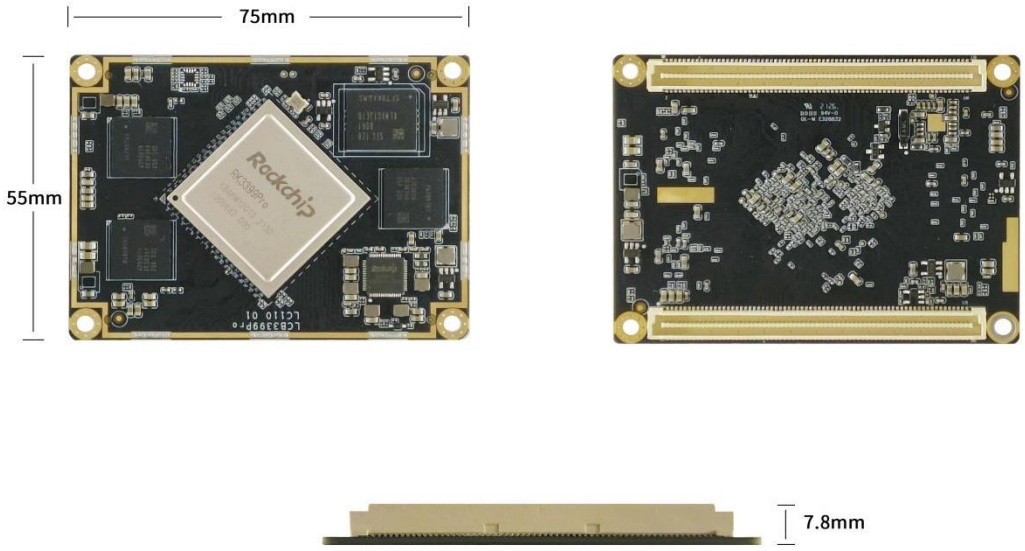
	Six on-chip SPI controllers
	Five on-chip UART controllers inside
	Nine on-chip I2C controllers
	Five groups of GPIO (GPIO0~GPIO4), totally have 122 GPIOs
	One PCIe port compatible with PCI Express V2.1 and dual operation mode （RC and EP）
	Six-channel single-ended 10-bit SAR-ADC up to 1MS/s sampling rate

Other Parameters

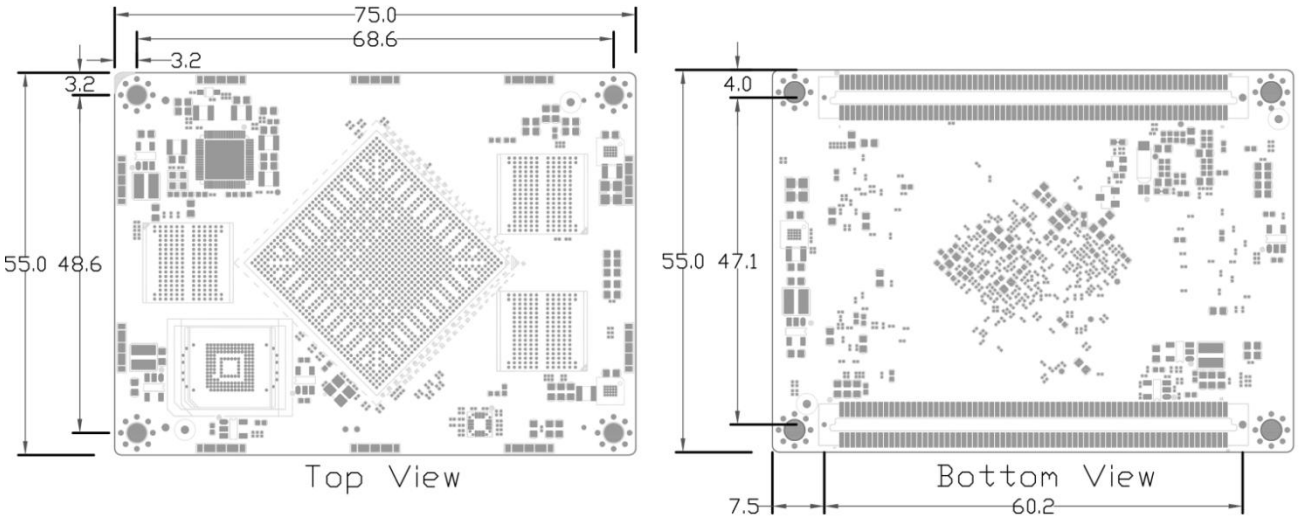
Operating temperature	Enterprise Grade: -20°C to 70°C
	Industrial Grade: -40°C to 85°C
PCB interface	B2B(280 Pin 0.8mm Pitch)
PCB layers	10 layers
PCB size	L* W *H(mm)：75 *55 * 7.8（PCB thickness 1.2mm）

4. Appearance and Dimensions

4.1 Appearance

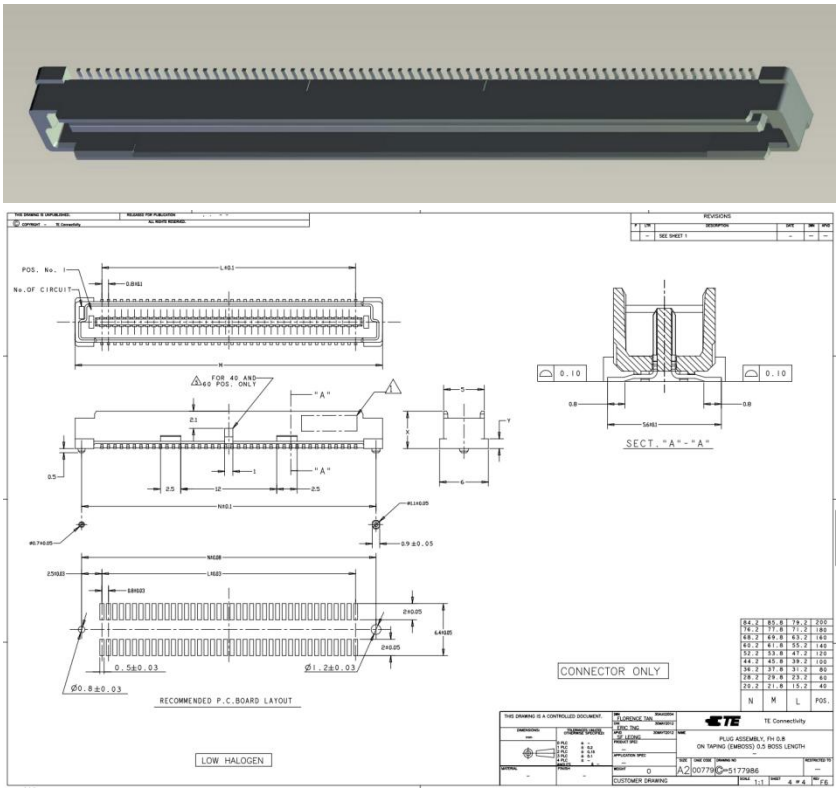


4.2 Dimensions

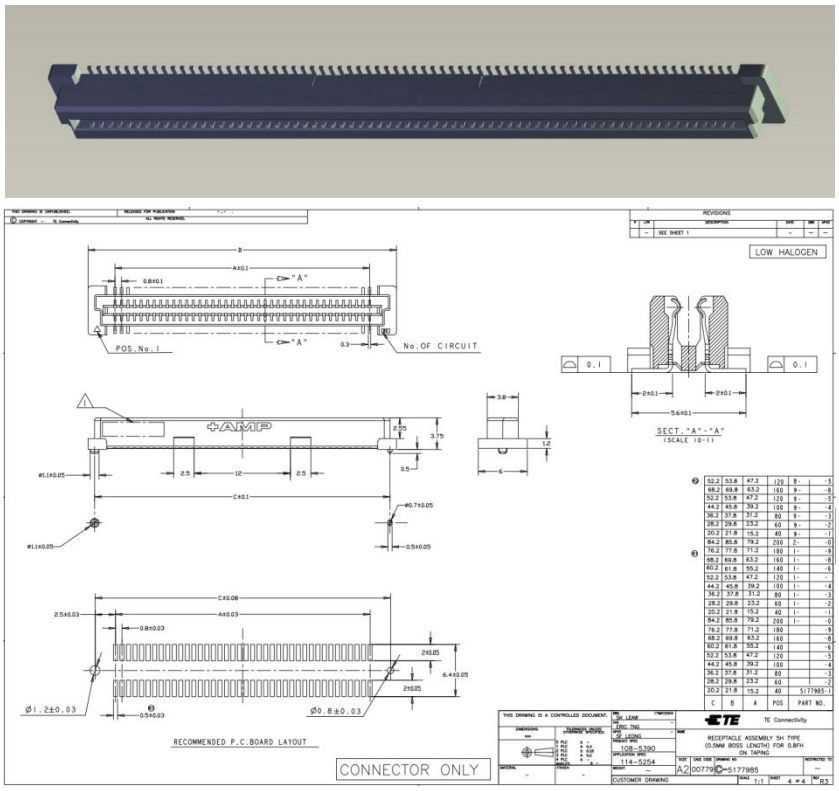


4.3 structure

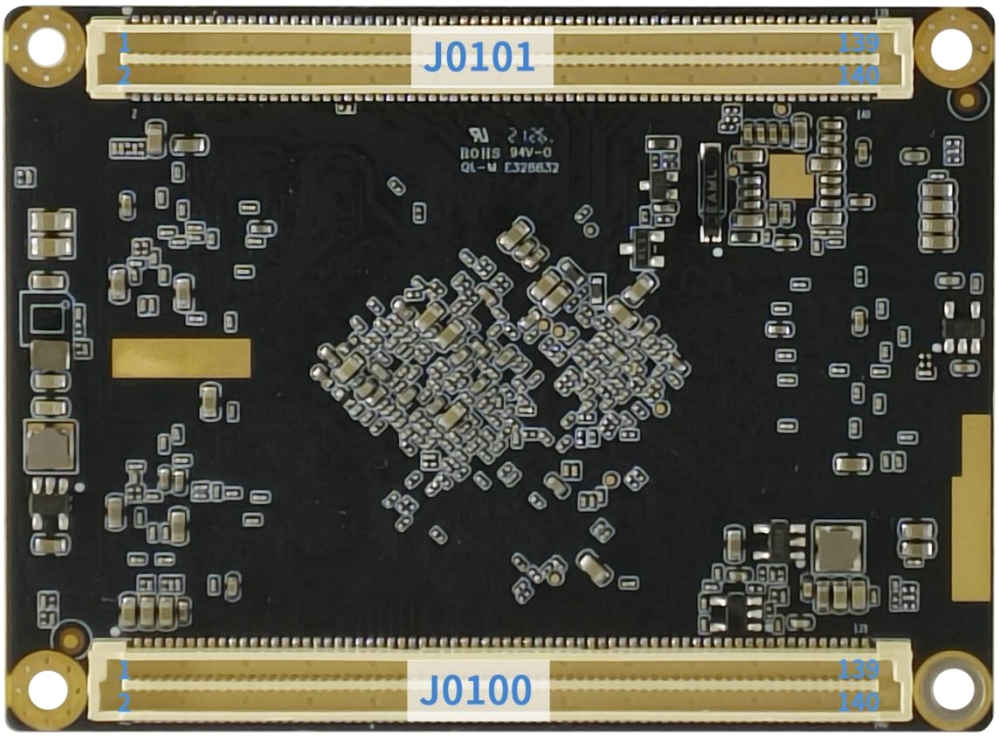
The LCB3399Pro utilizes two B2B connectors from Tyco Electronics/AMP, which are male headers with a 0.8mm pitch and a 2*70Pin configuration. The part number for these connectors is 5177986-6, as shown in the figure below.



The baseboard should select the corresponding female connector, with a standard combined height of 5mm. The part number for this connector is 5177985-6, as shown in the figure below.



5.Interface Definition



J100

Num	Pin Name	Pin Type	Default Type	I/O Pull	Description	Default Pin function	power domain
1	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A
2	GND	P	I	N/A	Main GND	Main power supply	N/A
3	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A
4	GND	P	I	N/A	Main GND	Main power supply	N/A
5	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A
6	GND	P	I	N/A	Main GND	Main power supply	N/A
7	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A
8	GND	P	I	N/A	Main GND	Main power supply	N/A
9	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A
10	GND	P	I	N/A	Main GND	Main power supply	N/A
11	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A
12	GND	P	I	N/A	Main GND	Main power supply	N/A
13	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A
14	GND	P	I	N/A	Main GND	Main power supply	N/A
15	VCC5V0_SYS_S3	P	I	N/A	Power input 5V/5A	Main power supply	N/A

16	GND	P	I	N/A	Main GND	Main power supply	N/A
	GPIO3_B2						APIO1
17	MAC_RXER	I/O	I	up	MAC receive error	No used for RGMII	-
	I2C5_SDA						(3.3V I/O)
18	VCCIO_3V3_S0	P	O	N/A	Power output 3.3V/0.5A	output for external devices IO supply	N/A
	GPIO3_B4						APIO1
19	MAC_TXEN	I/O	I	up	MAC transmit enable	PHY_TXEN	-
	UART1_RX						(3.3V I/O)
20	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
	GPIO3_A5						APIO1
21	MAC_TXD1	I/O	I	down	MAC transmit data	PHY_TXD1	-
	SPI0_TXD						(3.3V I/O)
22	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
	GPIO3_A1						APIO1
23	MAC_TXD3	I/O	I	down	MAC transmit data	PHY_TXD3	-
	SPI4_TXD						(3.3V I/O)
24	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
	GPIO3_A0						APIO1
25	MAC_TXD2	I/O	I	down	MAC transmit data	PHY_TXD2	-
	SPI4_RXD						(3.3V I/O)
26	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
	GPIO3_A4						APIO1
27	MAC_TXD0	I/O	I	down	MAC transmit data	PHY_TXD0	-
	SPI0_RXD						(3.3V I/O)
28	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
29	GND	P	N/A	N/A	N/A	N/A	N/A
30	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
	GPIO3_C1						APIO1
31	MAC_TXCLK	I/O	I	up	MAC transmit clock	PHY_TXCLK	-
	UART3_RTSN						(3.3V I/O)
32	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
33	GND	P	N/A	N/A	N/A	N/A	N/A
34	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
35	GPIO3_B3	I/O	I	up	MAC reference clock	MAC_CLK	APIO1

	MAC_CLK				output		-
	I2C5_SCL						(3.3V I/O)
36	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
37	GND	P	N/A	N/A	N/A	N/A	N/A
38	RFU	N/A	N/A	N/A	Reserve for future used	N/A	N/A
	GPIO3_B6						APIO1
39	MAC_RXCLK	I/O	I	up	MAC receive clock	MAC_RXCLK	-
	UART3_RX						(3.3V I/O)
	GPIO2_B4						APIO2
40	SPI2_CSN0	I/O	I	up	Camera power down control output for front	DVP_PDN0_H	-
	-						(1.8V I/O)
41	GND	P	N/A	N/A	N/A	N/A	N/A
42	GND	P	N/A	N/A	N/A	N/A	N/A
	GPIO3_A3						APIO1
43	MAC_RXD3	I/O	I	up	MAC receive data	MAC_RXD3	-
	SPI4_CSN0						(3.3V I/O)
44	EDP_AUXP	I/O	I/O	N/A	eDP AUX channel	eDP AUX channel	N/A
	GPIO3_B1						APIO1
45	MAC_RXDV	I/O	I	down	MAC receive data valid	MAC_RXDV	-
	-						(3.3V I/O)
46	EDP_AUXN	I/O	I/O	N/A	eDP AUX channel	eDP AUX channel	N/A
	GPIO3_A6						APIO1
47	MAC_RXD0	I/O	I	up	MAC receive data	MAC_RXD0	-
	SPI0_CLK						(3.3V I/O)
48	EDP_TX0P	I/O	O	N/A	eDP data lane	eDP data lane	N/A
	GPIO3_A7						APIO1
49	MAC_RXD1	I/O	I	up	MAC receive data	MAC_RXD1	-
	SPI0_CSN0						(3.3V I/O)
50	EDP_TX0N	I/O	O	N/A	eDP data lane	eDP data lane	N/A
51	GPIO3_A2	I/O	I	up	MAC receive data	MAC_RXD2	APIO1

	MAC_RXD2						-
	SPI4_CLK						(3.3V I/O)
52	EDP_TX1P	I/O	O	N/A	eDP data lane	eDP data lane	N/A
53	GPIO3_B5	I/O	I	up	MAC management command and data	MAC_MDIO	APIO1
	MAC_MDIO						-
	UART1_TX						(3.3V I/O)
54	EDP_TX1N	I/O	O	N/A	eDP data lane	eDP data lane	N/A
55	GPIO3_B0	I/O	I	up	MAC management clock	MAC_MDC	APIO1
	MAC_MDC						-
	SPI0_CSN1						(3.3V I/O)
56	EDP_TX2P	I/O	O	N/A	eDP data lane	eDP data lane	N/A
57	GPIO3_C0	I/O	I	up	MAC collision detect	PHY_INT	APIO1
	MAC_COL						-
	UART3_CTSN						(3.3V I/O)
	SPDIF_TX						-
58	EDP_TX2N	I/O	O	N/A	eDP data lane	eDP data lane	N/A
59	GPIO3_B7	I/O	I	up	MAC carrier sense detect	PHY_RST	APIO1
	MAC_CRS						-
	UART3_TX						(3.3V I/O)
	CIF_CLKOUTB						-
	-						-
	-						-
	-						-
60	EDP_TX3P	I/O	O	N/A	eDP data lane	eDP data lane	N/A
61	GND	P	N/A	N/A	N/A	N/A	N/A
62	EDP_TX3N	I/O	O	N/A	eDP data lane	eDP data lane	N/A
63	MIPI_MCLK	I/O	O	N/A	clock out for external devices	clock out for cameras	N/A
64	GND	P	N/A	N/A	N/A	N/A	N/A
65	GND	P	N/A	N/A	N/A	N/A	N/A
66	GPIO1_B3	I/O	I	up	I2C serial port 4,need external pull-up	I2C4_SDA	PMUIO2
	I2C4_SDA						-

	-						(1.8V I/O)
67	GPIO2_B3 SPI2_CLK VOP_DEN CIF_CLKOUTA	I/O	I	up	Camera clock output	CIF_CLK_OUT	APIO2 - (1.8V I/O) -
68	GPIO1_B4 I2C4_SCL -	I/O	I	up	I2C serial port 4,need external pull-up	I2C4_SCL	PMUIO2 - (1.8V I/O)
69	GPIO2_A5 VOP_D5 CIF_D5	I/O	I	down	Camera data port	CIF_D5	APIO2 - (1.8V I/O)
70	GPIO1_C5 I2C8_SCL -	I/O	I	up	I2C serial port 8,for CC,need external pull-up	I2C8_SCL_CC	PMUIO2 - (1.8V I/O)
71	GPIO2_B1 SPI2_RXD CIF_HREF I2C6_SDA	I/O	I	up	Camera href input	CIF_HREF	APIO2 - (1.8V I/O) -
72	GPIO1_C4 I2C8_SDA -	I/O	I	up	I2C serial port 8,for CC,need external pull-up	I2C8_SDA_CC	PMUIO2 - (1.8V I/O)
73	GPIO2_A6 VOP_D6 CIF_D6	I/O	I	down	Camera data port	CIF_D6	APIO2 - (1.8V I/O)
74	GPIO0_A3 SDIO0_WRPT -	I/O	I	down	WIFI module wake up AP	WIFI_HOST_WAKE_L	PMUIO1 - (1.8V I/O)
75	GPIO2_A0	I/O	I	up	Camera data port	CIF_D0	APIO2

	VOP_D0						-
	CIF_D0						(1.8V I/O)
	I2C2_SDA						-
	GPIO4_B5				SDMMC0 command output		SDMMC0
76	SDMMC0_CMD	I/O	I	up	JTAG TMS for MCU	SDMMC0_CMD	-
	MCUJTAG_TMS				-		(1.8V/3.0V auto)
	GPIO2_A7						APIO2
	VOP_D7						-
77	CIF_D7	I/O	I	up	Camera data port	CIF_D7	(1.8V I/O)
	I2C7_SDA						-
	GPIO4_B3				SDMMC0 data port		SDMMC0
78	SDMMC0_D3	I/O	I	up	JTAG TMS for AP	SDMMC0_D3/JTAG_TMS	-
	APJTAG_TMS				-		(1.8V/3.0V auto)
	GPIO2_A3						APIO2
79	VOP_D3	I/O	I	down	Camera data port	CIF_D3	-
	CIF_D3						(1.8V I/O)
	GPIO4_B1						SDMMC0
80	SDMMC0_D1	I/O	I	up	SDMMC0 data port	SDMMC0_D1/UART2_TX	-
	UART2A_TX						(1.8V/3.0V auto)
	GPIO2_A2						APIO2
81	VOP_D2	I/O	I	down	Camera data port	CIF_D2	-
	CIF_D2						(1.8V I/O)
	GPIO4_B4				SDMMC0 clock output		SDMMC0
82	SDMMC0_CLKOUT	I/O	I	down	JTAG TCK for MCU	SDMMC0_CLK	-
	MCUJTAG_TCK				-		(1.8V/3.0V auto)
	GPIO2_A4						
83	VOP_D4	I/O	I	down	Camera data port	CIF_D4	APIO2(1.8V I/O)
	CIF_D4						

	GPIO4_B0						SDMMC0
84	SDMMC0_D0	I/O	I	up	SDMMC0 data port	SDMMC0_D0/UART2_RX	-
	UART2A_RX						(1.8V/3.0V auto)
	GPIO2_B0						
	VOP_CLK						
85	CIF_VSYNC	I/O	I	up	Camera vsync input	CIF_VSYNC	APIO2(1.8V I/O)
	I2C7_SCL						
	GPIO4_B2				SDMMC0 data port		SDMMC0
86	SDMMC0_D2	I/O	I	up	JTAG TCK for AP	SDMMC0_D2/JTAG_TCK	-
	APJTAG_TCK				-		(1.8V/3.0V auto)
	GPIO2_A1						APIO2
	VOP_D1						-
87	CIF_D1	I/O	I	up	Camera data port	CIF_D1	(1.8V I/O)
	I2C2_SCL						-
	GPIO0_A7						PMUIO1
88	SDMMC0_DET	I/O	I	up	SDMMC0 detect input	SDMMC0_DET_L	-
	-						(1.8V I/O)
89	GND	P	N/A	N/A	N/A	N/A	N/A
	GPIO1_A2						PMUIO2
90	ISP0_FLASHTRIGIN	I/O	I	down	CC logic controler interrupt input	TYPEC_CC_INT_L	-
	ISP1_FLASHTRIGIN						(1.8V I/O)
	GPIO2_B2						APIO2
	SPI2_TXD						-
91	CIF_CLKIN	I/O	I	up	Camera clock input	CIF_CLKI	(1.8V I/O)
	I2C6_SCL						-
92	GND	P	N/A	N/A	N/A	N/A	N/A
93	GND	P	N/A	N/A	N/A	N/A	N/A
94	HOST1_DP	I/O	N/A	N/A	USB data port	USB data port	N/A
	GPIO0_B0						PMUIO1
95	SDMMC0_WRPT	I/O	I	up	N4 interrupt input	N4_INT_L	-
	TEST_CLKOUT2						(1.8V I/O)
96	HOST1_DM	I/O	N/A	N/A	USB data port	USB data port	N/A

	GPIO0_A1						PMUIO1
97	DDRIO_PWROFF	I/O	I	up	MIPI CAMERA RST	CAM_RST_L	-
	-						(1.8V I/O)
98	GND	P	N/A	N/A	N/A	N/A	N/A
99	GPIO0_B5	I/O	I	down	Headphone insert detect input	PHONE_DET_H	PMUIO1 - (1.8V I/O)
100	NPU_CIF_D4	I/O	I	down	NPU Camera data port	NPU_CIF_D4	NPU VCCIO2 - (1.8V IO)
101	GPIO0_B4	I/O	I	down	N4 reset output	N4_RST	PMUIO1 - (1.8V I/O)
102	NPU_CIF_D7	I/O	I	down	NPU Camera data port	NPU_CIF_D7	NPU VCCIO2 - (1.8V IO)
103	GPIO0_B1 PMUIO2_VOLSEL -	I/O	I	down	N4 power enable	N4_PWREN	PMUIO1 - (1.8V I/O)
104	NPU_CIF_D8	I/O	I	down	NPU Camera data port	NPU_CIF_D8	NPU VCCIO2 - (1.8V IO)
105	VCC_RTC_S5	P	I	N/A	Power input(5V/0.1A) for internal RTC	Power input(5V/0.1A) for internal RTC	N/A
106	NPU_CIF_D2	I/O	I	down	NPU Camera data port	NPU_CIF_D2	NPU VCCIO2 - (1.8V IO)
107	GPIO0_A5 EMMC_PWRON -	I/O	I	up	BT module wake up AP	BT_HOST_WAKE_L	PMUIO1 - (1.8V I/O)
108	NPU_CIF_D0	I/O	I	down	NPU Camera data port	NPU_CIF_PDN0	NPU VCCIO2

							-
							(1.8V IO)
109	GPIO1_B5	I/O	I	down	USB HOST power enable	USB5V0_EN_H	PMUIO2 - (1.8V I/O)
110	NPU_CIF_D3	I/O	I	down	NPU Camera data port	NPU_CIF_D3	NPU VCCIO2 - (1.8V IO)
111	GPIO1_B0 SPI1_TXD UART4_TX	I/O	I	up	Reserve	Reserve	PMUIO2 - (1.8V I/O)
112	NPU_CIF_HREF	I/O	I	down	Camera href input	NPU_CIF_HREF	NPU VCCIO2 - (1.8V IO)
113	GPIO1_B2 SPI1_CSN0 PMCU_JTAG_TMS	I/O	I	up	Reserve	Reserve	PMUIO2 - (1.8V I/O)
114	NPU_CIF_D5	I/O	I	down	NPU Camera data port	NPU_CIF_D5	NPU VCCIO2 - (1.8V IO)
115	GPIO1_A7 SPI1_RXD UART4_RX	I/O	I	up	Reserve	Reserve	PMUIO2 - (1.8V I/O)
116	GND	P	N/A	N/A	N/A	N/A	N/A
117	GPIO1_B1 SPI1_CLK PMCU_JTAG_TCK	I/O	I	up	Reserve	Reserve	PMUIO2 - (1.8V I/O)
118	NPU_CIF_CLKOUT	I/O	I	down	Camera clock output	NPU_CIF_CLKOUT	NPU VCCIO2 - (1.8V IO)
119	GPIO0_A6 PWM3A_IR	I/O	I	down	IR receiver input	IR_RX	PMUIO1 -

	-						(1.8V I/O)
120	GND	P	N/A	N/A	N/A	N/A	N/A
121	GND	P	N/A	N/A	N/A	N/A	N/A
122	NPU_CIF_CLKIN	I/O	I	down	Camera clock input	NPU_CIF_CLKIN	NPU VCCIO2 - (1.8V IO)
123	VCC3V3_SYS_S3	P	O	N/A	Power output(3.3V/1A) for external devices	Power output(3.3V/1A) for external devices	N/A
124	GND	P	N/A	N/A	N/A	N/A	N/A
125	VCC3V3_SYS_S3	P	O	N/A	Power output(3.3V/1A) for external devices	Power output(3.3V/1A) for external devices	N/A
126	NPU_CIF_D10	I/O	I	down	NPU Camera data port	NPU_CIF_RST	NPU VCCIO2 - (1.8V IO)
127	VCC_BUCK5_S3	P	O	N/A	Power output(2.3V/1A) for external devices	Power output(3.3V/1A) for external devices	N/A
128	NPU_CIF_D1	I/O	I	down	NPU Camera data port	NPU_CIF_PDN1	NPU VCCIO2 - (1.8V IO)
129	VCC_BUCK5_S3	P	O	N/A	Power output(2.3V/1A) for external devices	Power output(3.3V/1A) for external devices	N/A
130	NPU_CIF_D6	I/O	I	down	NPU Camera data port	NPU_CIF_D6	NPU VCCIO2 - (1.8V IO)
131	ADC_IN4	A	N/A	N/A	SAR-ADC input channel4	Reserve	SAR ADC - (1.8V ADC)
132	NPU_CIF_D11	I/O	I	down	NPU Camera data port	NPU_CIF_PWREN_H	NPU VCCIO2 - (1.8V IO)
133	ADC_IN1	A	N/A	N/A	SAR-ADC input channel1	Reserve	SAR ADC - (1.8V ADC)
134	NPU_CIF_VSYNC	I/O	I	down	Camera vsync input	NPU_CIF_VSYNC	NPU VCCIO2

							– (1.8V IO)
135	ADC_IN2	A	N/A	N/A	AD Key Array input	ADC2_KEY_IN	SAR ADC – (1.8V ADC)
136	NPU_CIF_D9	I/O	I	down	NPU Camera data port	NPU_CIF_D9	NPU VCCIO2 – (1.8V IO)
137	ADC_IN3	A	N/A	N/A	Headphone MIC input	ADC3_HP_HOOK	SAR ADC – (1.8V ADC)
138	NPU_I2C3_SCL	I/O	I	up	NPU I2C serial port 3,for Camera,need external pull-up	NPU_I2C3_SCL	NPU VCCIO2 – (1.8V IO)
139	ADC_IN0	A	N/A	N/A	SAR-ADC input channel0	Reserve	SAR ADC – (1.8V ADC)
140	NPU_I2C3_SDA	I/O	I	up	NPU I2C serial port 3,for Camera,need external pull-up	NPU_I2C3_SDA	NPU VCCIO2 – (1.8V IO)

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Num	Pin Name	Pin Type	Default Type	I/O Pull	Description	Default Pin function	power domain
1	GPIO3_D3 I2S0_SDI0 –	I/O	I	down	I2S 0 port, for MIC Array	Reserve for MIC Array	APIO5 – (1.8V I/O)
2	GPIO4_C6 PWM1 –	I/O	I	down	Touch panel reset output	TOUCH_RST_L	APIO4 – (3.0V IO)

3	GPIO3_D5 I2S0_SDI2SDO2 -	I/O	I	down	I2S 0 port, for MIC Array	Reserve for MIC Array	APIO5 - (1.8V I/O)
4	GPIO4_A1 I2C1_SDA -	I/O	I	up	I2C serial port 1,for Audio,need external pull-up	I2C1_SDA_1V8	APIO5 - (1.8V I/O)
5	GPIO3_D0 I2S0_SCLK -	I/O	I	down	I2S 0 port, for MIC Array	Reserve for MIC Array	APIO5 - (1.8V I/O)
6	GPIO4_A2 I2C1_SCL -	I/O	I	up	I2C serial port 1,for Audio,need external pull-up	I2C1_SCL_1V8	APIO5 - (1.8V I/O)
7	GPIO4_D2	I/O	I	down	Reserve	Reserve	APIO4 - (3.0V IO)
8	GPIO4_D6	I/O	I	down	LCD power enable	LCD_EN	APIO4 - (3.0V IO)
9	GPIO3_D6 I2S0_SDI3SDO1 -	I/O	I	down	I2S 0 port, for MIC Array	Reserve for MIC Array	APIO5 - (1.8V I/O)
10	GPIO4_C0 I2C3_SDA UART2B_RX	I/O	I	up	I2C serial port 3,for HDMI,need external pull-up	I2C3_SDA_HDMI	APIO4 - (3.0V IO)
11	GPIO3_D7 I2S0_SDO0 -	I/O	I	down	Compass interrupt input	COMP_INT_H	APIO5 - (1.8V I/O)
12	GPIO4_C1	I/O	I	up	I2C serial port 3,for	I2C3_SCL_HDMI	APIO4

	I2C3_SCL				HDMI,need external pull-up		-
	UART2B_TX						(3.0V IO)
13	GPIO4_D0	I/O	I	up	Reserve	Reserve	APIO4
	PCIE_CLKREQNB						-
	-						(3.0V IO)
14	GPIO4_C4	I/O	I	up	TOUCH power control output	TOUCH_PWR_EN_H	APIO4
	UART2C_TX						-
	-						(3.0V IO)
15	GPIO3_D1	I/O	I	down	I2S 0 port, for MIC Array	Reserve for MIC Array	APIO5
	I2S0_LRCK_RX						-
	-						(1.8V I/O)
16	GPIO4_C3	I/O	I	up	TOUCH interrupt input	TOUCH_INT_L	APIO4
	UART2C_RX						-
	-						(3.0V IO)
17	GPIO3_D2	I/O	I	down	G-sensor interrupt input	GSENSOR_INT_L	APIO5
	I2S0_LRCK_TX						-
	-						(1.8V I/O)
18	GPIO2_D2	I/O	I	up	AP wake up BT module	BT_WAKE_L	APIO3 (1.8V I/O)
	SDIO0_DETN						
	PCIE_CLKREQN						
19	GPIO3_D4	I/O	I	down	I2S 0 port, for MIC Array	Reserve for MIC Array	APIO5
	I2S0_SDI1SDO3						-
	-						(1.8V I/O)
20	GPIO4_D1	I/O	I	down	USB2.0 HUB reset output	USB20_HUB_RESET	APIO4
	DP_HOTPLUG						-
	-						(3.0V IO)
21	GPIO4_D5	I/O	I	down	Reserve	Reserve	APIO4

							-
							(3.0V IO)
22	GPIO2_C1 UART0_TX	I/O	I	up	UART0 serial port, for BT module	UART0_TXD_BT	APIO3 (1.8V I/O)
23	GPIO4_C5 SPDIF_TX -	I/O	I	down	USB Type-C0 power control output	VCC5V0_TYPEC0_EN	APIO4 - (3.0V IO)
24	GPIO2_D4 SDIO0_BKPWR	I/O	I	down	BT module power enable	BT_REG_ON_H	APIO3 (1.8V I/O)
25	GND	P	N/A	N/A	N/A	N/A	N/A
26	GPIO2_C2 UART0_CTSN	I/O	I	up	UART0 serial port, for BT module	UART0_CTS_BT	APIO3 (1.8V I/O)
27	MIPI_TX1 RX1_D0N	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
28	GPIO4_D4	I/O	I	down	Camera power down control output for rear	DVP_PDN1_3V3	APIO4 - (3.0V IO)
29	MIPI_TX1 RX1_D0P	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
30	GPIO2_C3 UART0_RTSN	I/O	I	up	UART0 serial port, for BT module	UART0_RTS_BT	APIO3 (1.8V I/O)
31	MIPI_TX1 RX1_D1N	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
32	GPIO4_C2 PWM0 VOP0_PWM VOP1_PWM	I/O	I	down	LCD panel backlight brightness control output	LCD_BL_PWM	APIO4 - (3.0V IO) -
33	MIPI_TX1 RX1_D1P	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
34	GPIO4_C7 HDMI_CECINOUT EDP_HOTPLUG	I/O	I	up	HDMI CEC communication	HDMI_CEC	APIO4 - (3.0V IO)
35	GND	P	N/A	N/A	N/A	N/A	N/A
36	MIC1_IN	A	I	N/A	Microphone channel 1 input	Microphone channel 1 input	N/A
37	MIPI_TX1	I/O	N/A	N/A	MIPI-DSI1/CSI1 clock	MIPI-DSI1/CSI1 clock lane	N/A

	RX1_CLKN				lane		
38	MIC2_IN	A	I	N/A	Microphone channel 2 input	Microphone channel 2 input	N/A
39	MIPI_TX1 RX1_CLKP	I/O	N/A	N/A	MIPI-DSI1/CSI1 clock lane	MIPI-DSI1/CSI1 clock lane	N/A
40	HPR	A	O	N/A	Headphone right channel output	Headphone right channel output	N/A
41	GND	P	N/A	N/A	N/A	N/A	N/A
42	HP_SNS	A	O	N/A	Headphone GND output	Headphone GND output	N/A
43	MIPI_TX1 RX1_D2N	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
44	HPL	A	O	N/A	Headphone left channel output	Headphone left channel output	N/A
45	MIPI_TX1 RX1_D2P	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
46	GND	P	N/A	N/A	N/A	N/A	N/A
47	MIPI_TX1 RX1_D3N	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
48	MIPI_TX0_D3N	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A
49	MIPI_TX1 RX1_D3P	I/O	N/A	N/A	MIPI-DSI1/CSI1 data lane	MIPI-DSI1/CSI1 data lane	N/A
50	MIPI_TX0_D3P	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A
51	GND	P	N/A	N/A	N/A	N/A	N/A
52	MIPI_TX0_D2P	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A
53	HDMI_TXCN	/O	N/A	N/A	HDMI clock lane	HDMI clock lane	N/A
54	MIPI_TX0_D2N	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A
55	HDMI_TXCP	/O	N/A	N/A	HDMI clock lane	HDMI clock lane	N/A
56	GND	P	N/A	N/A	N/A	N/A	N/A
57	HDMI_TX0N	/O	N/A	N/A	HDMI data lane	HDMI data lane	N/A
58	MIPI_TX0_CLKN	I/O	N/A	N/A	MIPI-DSI0 clock lane	MIPI-DSI0 clock lane	N/A
59	HDMI_TX0P	/O	N/A	N/A	HDMI data lane	HDMI data lane	N/A
60	MIPI_TX0_CLKP	I/O	N/A	N/A	MIPI-DSI0 clock lane	MIPI-DSI0 clock lane	N/A
61	HDMI_TX1N	/O	N/A	N/A	HDMI data lane	HDMI data lane	N/A
62	GND	P	N/A	N/A	N/A	N/A	N/A
63	HDMI_TX1P	/O	N/A	N/A	HDMI data lane	HDMI data lane	N/A
64	MIPI_TX0_D1P	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A
65	HDMI_TX2N	/O	N/A	N/A	HDMI data lane	HDMI data lane	N/A
66	MIPI_TX0_D1N	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A
67	HDMI_TX2P	/O	N/A	N/A	HDMI data lane	HDMI data lane	N/A
68	MIPI_TX0_D0N	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A
69	GND	P	N/A	N/A	N/A	N/A	N/A
70	MIPI_TX0_D0P	I/O	N/A	N/A	MIPI-DSI0 data lane	MIPI-DSI0 data lane	N/A

71	TYPEC0_RX1N	/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data receive	USB3.0 PHY0 SuperSpeed differential data receive	N/A
72	GND	P	N/A	N/A	N/A	N/A	N/A
73	TYPEC0_RX1P	/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data receive	USB3.0 PHY0 SuperSpeed differential data receive	N/A
74	TYPEC0_SBU1	I/O	N/A	N/A	TYPEC0 AUX differential TX/RX serial data	TYPEC0 AUX differential TX/RX serial data	N/A
75	TYPEC0_TX1P	I/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data transmit	USB3.0 PHY0 SuperSpeed differential data transmit	N/A
76	TYPEC0_SBU2	I/O	N/A	N/A	TYPEC0 AUX differential TX/RX serial data	TYPEC0 AUX differential TX/RX serial data	N/A
77	TYPEC0_TX1N	I/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data transmit	USB3.0 PHY0 SuperSpeed differential data transmit	N/A
78	GND	P	N/A	N/A	N/A	N/A	N/A
79	TYPEC0_RX2N	/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data receive	USB3.0 PHY0 SuperSpeed differential data receive	N/A
80	TYPEC0_DM	I/O	N/A	N/A	USB2.0 OTG0 Data port	USB2.0 OTG0 Data port	N/A
81	TYPEC0_RX2P	/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data receive	USB3.0 PHY0 SuperSpeed differential data receive	N/A
82	TYPEC0_DP	I/O	N/A	N/A	USB2.0 OTG0 Data port	USB2.0 OTG0 Data port	N/A
83	TYPEC0_TX2P	I/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data transmit	USB3.0 PHY0 SuperSpeed differential data transmit	N/A
84	GND	P	N/A	N/A	N/A	N/A	N/A
85	TYPEC0_TX2N	I/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data transmit	USB3.0 PHY0 SuperSpeed differential data transmit	N/A
86	USB20_OTG1_DM	I/O	N/A	N/A	USB2.0 OTG1 Data port	USB2.0 OTG1 Data port	N/A
87	GND	P	N/A	N/A	N/A	N/A	N/A
88	USB20_OTG1_DP	I/O	N/A	N/A	USB2.0 OTG1 Data port	USB2.0 OTG1 Data port	N/A
89	USB30_RX1M	/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential data receive	USB3.0 PHY0 SuperSpeed differential data receive	N/A
90	GND	P	N/A	N/A	N/A	N/A	N/A
91	USB30_RX1P	/O	N/A	N/A	USB3.0 PHY0 SuperSpeed differential	USB3.0 PHY0 SuperSpeed differential data receive	N/A

					data receive		
92	HDMI_PORT_HPD	I/O	N/A	N/A	HDMI Hot Plug Detection interrupt with 5V tolerance	HDMI Hot Plug Detection interrupt with 5V tolerance	N/A
93	USB30_TX1P	/O	N/A	N/A	USB3.0 PHY1 SuperSpeed differential data transmit	USB3.0 PHY1 SuperSpeed differential data transmit	N/A
94	GND	P	N/A	N/A	N/A	N/A	N/A
95	USB30_TX1M	/O	N/A	N/A	USB3.0 PHY1 SuperSpeed differential data transmit	USB3.0 PHY1 SuperSpeed differential data transmit	N/A
96	TYPEC0_SBU2_DC	I/O	N/A	N/A	TYPEC0 AUX pull-up/pull-down polarity reversal pins	TYPEC0 AUX pull-up/pull-down polarity reversal pins	N/A
97	GND	P	N/A	N/A	N/A	N/A	N/A
98	TYPEC0_SBU1_DC	I/O	N/A	N/A	TYPEC0 AUX pull-up/pull-down polarity reversal pins	TYPEC0 AUX pull-up/pull-down polarity reversal pins	N/A
99	NPU_MIPI_RX_D3P	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A
100	GND	P	N/A	N/A	N/A	N/A	N/A
101	NPU_MIPI_RX_D3N	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A
102	TYPEC0_U2VBUSDET	I/O	N/A	N/A	USB2.0 OTG0 inserted detect	USB2.0 OTG0 inserted detect	N/A
103	GND	P	N/A	N/A	N/A	N/A	N/A
104	TYPEC0_ID	I/O	N/A	N/A	TYPEC0 ID detect input	TYPEC0 ID detect input	N/A
105	NPU_MIPI_RX_CLKP	I/O	N/A	N/A	NPU MIPI-CSI differential clock lane	NPU MIPI-CSI differential clock lane	N/A
106	GND	P	N/A	N/A	N/A	N/A	N/A
107	NPU_MIPI_RX_CLKN	I/O	N/A	N/A	NPU MIPI-CSI differential clock lane	NPU MIPI-CSI differential clock lane	N/A
108	NPU_MIPI_RX_D2P	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A
109	GND	P	N/A	N/A	N/A	N/A	N/A
110	NPU_MIPI_RX_D2N	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A
111	NPU_MIPI_RX_D1N	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A
112	GPIO2_D3 SDIO0_PWREN	I/O	I	down	WIFI module power enable	WIFI_REG_ON_H	APIO3 (1.8V I/O)
113	NPU_MIPI_RX_D1P	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A

							NPU VCCIO6
114	NPU_UART2_TX	I/O	I	up	NPU UART2 serial port, for NPU debug	Test Point	-
							(3.3V IO)
115	NPU_MIPI_RX_D0N	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A
							NPU VCCIO6
116	NPU_UART2_RX	I/O	I	up	NPU UART2 serial port, for NPU debug	Test Point	-
							(3.3V IO)
117	NPU_MIPI_RX_D0P	I/O	N/A	N/A	NPU MIPI-CSI differential data lane	NPU MIPI-CSI differential data lane	N/A
							PMUIO2
118	32K_OUT	I/O	O	up	32768HZ clock output	32768HZ clock output	-
							(1.8V I/O)
119	GND	P	N/A	N/A	N/A	N/A	N/A
120	VCCIO_3V0_S0	P	O	N/A	Power output (3.0V/0.3A) for external devices IO supply	Power output (3.0V/0.3A) for external devices IO supply	N/A
121	VCC3V0_SD_S0	P	O	N/A	Power output (3.0V/0.4A) for SD card	Power output (3.0V/0.4A) for SD card	N/A
122	EXT_PWR_EN	I/O	O	N/A	external DC-DC enable signal output	external DC-DC enable signal output	N/A
	GPIO2_C4						APIO3
123	SDIO0_D0	I/O	I	up	SDIO0 data port ,for WIFI module	SDIO0_D0	-
	SPI5_RXD						(1.8V I/O)
							PMUIO2
124	SYS_RST	I/O		up	CPU reset signal input	CPU reset signal input	-
							(1.8V I/O)
	GPIO2_D0						APIO3
125	SDIO0_CMD	I/O	I	up	SDIO0 command output,for WIFI module	SDIO0_CMD	-
	-						(1.8V I/O)
	GPIO2_C7						APIO3
126	SDIO0_D3	I/O	I	up	SDIO0 data port ,for WIFI module	SDIO0_D3	-
	SPI5_CSN0						(1.8V I/O)
127	GND	P	N/A	N/A	N/A	N/A	N/A
128	GPIO2_C5	I/O	I	up	SDIO0 data port ,for	SDIO0_D1	APIO3

	SDIO0_D1			WIFI module		-
	SPI5_TXD					(1.8V I/O)
	GPIO2_D1					APIO3
129	SDIO0_CLKOUT	I/O	I	up	SDIO0 clock output,for WIFI module	SDIO0_CLK	-
	TEST_CLKOUT1					(1.8V I/O)
	GPIO2_C6					APIO3
130	SDIO0_D2	I/O	I	up	SDIO0 data port ,for WIFI module	SDIO0_D2	-
	SPI5_CLK					(1.8V I/O)
131	GND	P	N/A	N/A	N/A	N/A	N/A
	GPIO2_C0					APIO3
132	UART0_RX	I/O	I	up	UART0 serial port, for BT module	UART0_RXD_BT	-
	-					(1.8V I/O)
133	KEY_PWR_ON	I/O	I	up	power on signal input	power on signal input	VCC_RTC_S5
134	VCC_1V8_S3	P	O	N/A	Power output(1.8V/0.3A) for external devices IO supply	Power output(1.8V/0.3A) for external devices IO supply	N/A
135	DCIN_PWR_ON	P	I	N/A	Adapter voltage detect input	Adapter voltage detect input	N/A
136	GND	P	N/A	N/A	N/A	N/A	N/A
137	VCC_1V8_S0	P	O	N/A	Power output(1.8V/0.3A) for external devices IO supply	Power output(1.8V/0.3A) for external devices IO supply	N/A
138	SPKN_OUT	A	O	N/A	speaker output signal	speaker output signal	N/A
139	VCC1V8_DVP_S0	P	O	N/A	Power output(1.8V/0.3A) for external devices IO supply	Power output(1.8V/0.3A) for external devices IO supply	N/A
140	SPKP_OUT	A	O	N/A	speaker output signal	speaker output signal	N/A

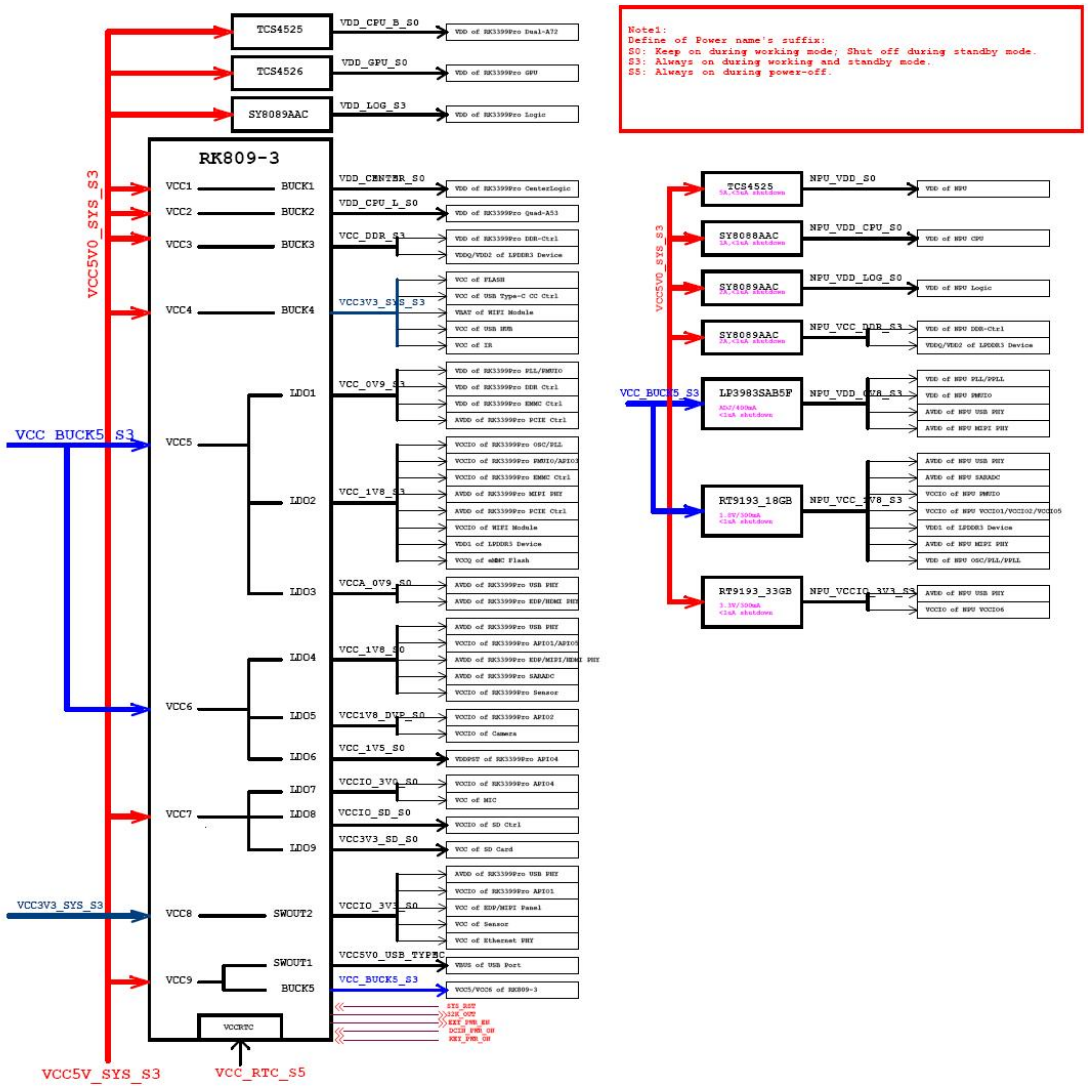
Notes1:

①:Pin Type: I = input, O = output, I/O = input/output (bidirectional), P=power supply, A = Analog input

② :I/O Pull: u=default pull-up, d=default pull-down, Z=default high-Z, fix up=default pull-up and can't be configured to pull-down

③:Output Drive Unit is mA, only Digital IO has driver strength value;

Power Supply Topology Diagram



power-on conditions

VCC_RTC_S5 voltage should be higher than 4.8V.

VCC5V0_SYS_S3 provides a 5V voltage and a current of more than 4A.

DCIN_PWR_ON serves as a forced power-on signal; when its voltage is above 4.8V, the system powers on and cannot be shut down by the Power_Key button. When DCIN_PWR_ON is left floating, the system can be powered on via the Power_Key button press, and the system will power on when this signal is pulled low for more than 500ms.

6.Application Scenarios

AI

Machine Vision

Industrial Control

Energy and Power

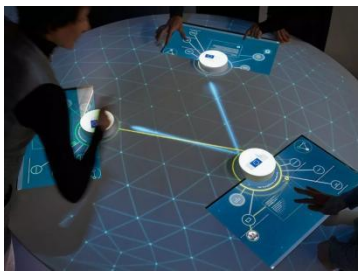
Smart Tablet

VR

Smart Logistics

New

Smart Commercial



Object Recognition

Vehicle terminal

Security Surveillance

7.Ordering Model

Product Model	Status	CPU	DDR	eMMC	Operating Temperature
LC11031600	ACTIVE	RK3399Pro	3GB	16GB	-10℃ - 70℃
LC11061600	ACTIVE	RK3399Pro	6GB	16GB	-10℃ - 70℃
LC11066400	ACTIVE	RK3399Pro	6GB	64GB	-10℃ - 70℃

*For customized non-standard orders, please contact us via email at sales@neardi.com.

8.About Neardi

Shanghai Neardi Technology Co., Ltd., established in 2014, is a national-level high-tech enterprise, a strategic partner of Rockchip, and an authorized agent for Black Sesame Technologies. We focus on the research and development and production of enterprise-level open-source hardware platforms, offering customers core modules, industry-specific boards, development boards, touch panels, and industrial control hosts. Adhering to the core philosophy of technological innovation and professional service, leveraging Neardi Technology's technical strengths and industry experience, we assist our partners in achieving rapid mass production of their products.

Company Advantages

Software Design / Custom OS / Product ODM / Bulk Delivery

Products

Rockchip

System On Module


LCB3588/J


LCB3568/J


LCB3566


LCB3399Pro


LCB3399

Development Board


LKD3588/J


LKD3568/J


LKD3566


LKD3399Pro


LKD3399

Embedded Computer


LPB3588


LPM3588


LPC3588


LPB3568


LPB3399Pro

Black Sesame Technologies


SOM-A-A1000


SOM-π-A1000


SOM-B-A1000


SOM-A1000 开发者套件

Vehicle Terminal


LPA3588


LPA3568


LPA3399Pro


LPS3399Pro

WIFI Module

FD7352S

FD7352P

FD7352M

FD7155U

FD7256S